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RENESAS TECHNICAL UPDATE

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Title	RX610 Group Notes on DMAC/DTC transfer using Communication Function		Information Category	Technical Notification		
Applicable Product	RX610 Group	Lot No. All lots	Reference Document	RX610 Group Hardware Manual		

Thank you for your consistent patronage of Renesas semiconductor products.

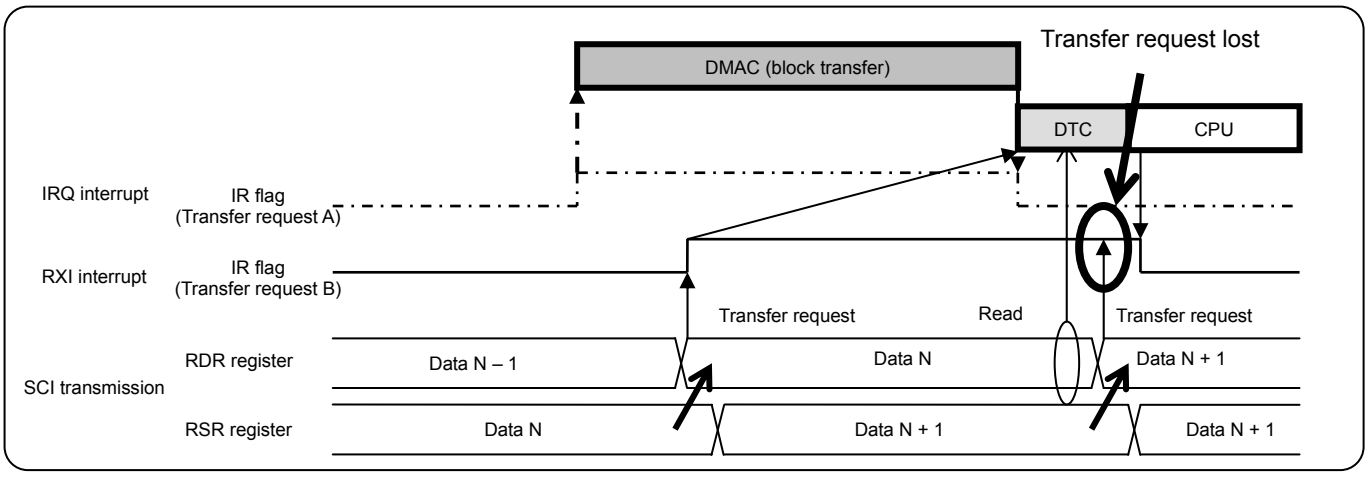
We would like to inform you of notes on DMAC/DTC transfer in the RX610 group.

1. Notes on transferring DMAC/DTC using Communication Function (SCI, RIIC)

When the DMAC/DTC is activated using an interrupt from the communication function, the DMAC/DTC cannot accept an activation request from the communication function and may not perform DMAC/DTC transfer. In this phenomenon, when the next transfer request is issued by the time that the interrupt status flag (IR flag) is automatically cleared after data transfer (reading reception data or writing Transmit data) using the DMAC/DTC, the transfer request is lost.

For example, when the DTC is activated using the SCI reception interrupt with CPU interrupt (DISEL=1) for every transfer, the IR flag is set to 1 in a first receiving operation and the DTC is activated. After the DTC transfer, the IR flag is retained at 1 until the CPU interrupt is received. In the meantime, if a second receiving operation is completed, a setting of the IR flag that is the transfer request is ignored. Therefore, the DTC cannot be activated, and the data received in second receiving operation cannot be transferred.

Example) SCI reception + DTC transfer (CPU interrupt (DISEL = 1) for every transfer), a DMAC block transfer using the IRQ interrupt



The following table shows setting conditions of the DMAC/DTC and occurrence of the phenomenon.

Destination of interrupt request from communication function	Chain Transfer Used or Not Used	No	Communication Interrupts to CPU Issued or Not Issued *1	Possibility of problem occurrence
DMAC	- (Chain transfer not provided)	1	No CPU interrupt (ISEL[1:0]=10b)	Impossible
		2	CPU interrupt (ISEL[1:0]=11b)	Possible
DTC	Chain transfer not used	3	No CPU interrupt (DISEL=0)	Impossible *2
		4	CPU interrupt (DISEL=1)	Possible
	Chain transfer used	5	No CPU interrupt (DISEL=0)	Impossible *2
		6	CPU interrupt (DISEL=1)	Possible

Note 1: Communication Interrupts include: transmit data empty and receive data full interrupts from SCI and RIIC.

Note 2: In the final transfer, if the DTC is re-set too late for the transfer request of the next packet to be transmitted/received, the same problem may occur as with the case in DESEL = 1.

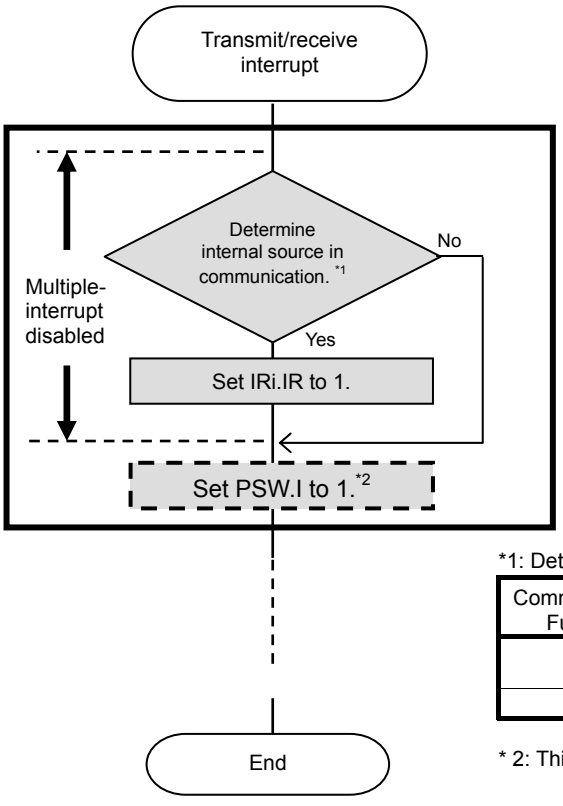
・When the DMAC is used with ISEL[1:0] ＝ 11b, use the DTC with DISEL = 1 and implement the following preventive measures.

・When the DTC is used with DISEL = 1, it should be used such that the transfer request is not lost, or implement the software preventive measures of the DTC to prevent the transfer request from being lost.

2. Software Preventive Measures

The flowchart for software preventive measures to be taken for the DTC is shown below. *

The flowchart for measures with DISEL=1



Addition (Software preventive measures)

*1: Determination of Internal Source in Communication

Communication Function	Receive buffer full flag	Transmit buffer empty flag	Remarks
SCI	SSR.RDRF=1	SSR.TDRE=1	See next page
RIIC	ICSR2.RDRF=1	ICSR2.TDRE=1	—

* 2: This step is not required when multiple-interrupt is not used.

3. Specifications Addition Disclosure

Following specifications are disclosed for the software preventive measures to be taken this time.

3.1 Add following specifications in bits 7 and 6 in SSR (Serial Status Register) of SCI.

Existing Specification

b7	b6	b5	b4	b3	b2	b1	b0
—	—	ORER	FER	PER	TEND	—	—
×	×	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b1-b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b2	TEND	Transmit Flag End	0: A character is being transmitted. 1: Character transfer has been completed	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error has occurred	R/(W)*
b4	FER	Framing Error Flag	: Framing error has not occurred 1: Framing error has occurred	R/(W)*
b5	ORER	Overrun Error Flag	0: No overrun error occurred 0 1: An overrun error has occurred	R/(W)*
b7-b6	-	Reserved	The read value is undefined. The write value should always be 1.	R/W

Note: Only 0 can be written to this bit, to clear the flag, after reading 1.

Specification update

b7	b6	b5	b4	b3	b2	b1	b0
TDRE	RDRF	ORER	FER	PER	TEND	—	—
1	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b1-b0	—	Reserved	These bits are always read as 0. The write value should always be 0.	R/W
b2	TEND	Transmit End Flag	0: A character is being transmitted. 1: Character transfer has been completed.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: A parity error has occurred	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: A framing error has occurred	R/(W)*1
b5	ORER	Overrun Error Flag	0: Overrun error has not occurred 1: Overrun error has occurred	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: When data is transferred from RDR 1: When data has been received normally, and transferred from RSR to RDR	R/(W)*2
b7	TDRE	Transmit Data Empty Flag	0: When data is transferred to TDR 1: When data is transferred from TDR to TSR	R/(W)*2

Notes: 1. Only 0 can be written to this bit, to clear the flag, after reading 1.
2. Write 1 when writing is necessary.

3.2 Add following specifications in IR flag in IRi (Interrupt Request Register) of ICU.

Existing Specification

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	IR
0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IR	Interrupt Status Flag	0: No interrupt request is generated. 1: An interrupt request is generated.	R/(W)*
b7-b1	-	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note: For edge-detected sources, only writing 0 to clear the flag is possible. Writing 1 is prohibited. For level-detected sources, writing is impossible.

Specification update

b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	IR
0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	IR	Interrupt Status Flag	0: No interrupt request is generated. 1: An interrupt request is generated.	R/(W)*
b7-b1	-	Reserved	These bits are always read as 0. The write value should always be 0.	R/W

Note: For edge-detected sources, only writing 0 to clear the flag is possible. Writing 1 is prohibited except when 1 is written to prevent loss of DTC transfer requests through software. For level-detected sources, writing is impossible.

4. Modifications in IO header file (iodefine.h)

Modify the IO header file, as shown below, according to the specifications added.

[Before modification]

```
struct st_sci0 {
・・・
 unsigned char TDR;
   union {
      unsigned char BYTE;
      struct {
         unsigned char :2;
         unsigned char ORER:1;
         unsigned char FER:1;
         unsigned char PER:1;
         unsigned char TEND:1;
         unsigned char :2;
      } BIT;
      struct {
         unsigned char :2;
         unsigned char ORER:1;
         unsigned char ERS:1;
         unsigned char PER:1;
         unsigned char TEND:1;
         unsigned char :2;
      } BIT2;
   } SSR;
   unsigned char RDR;
・・・
```

[After modification]

```
struct st_sci0 {
・・・
 unsigned char TDR;
   union {
      unsigned char BYTE;
      struct {
         unsigned char TDRE:1;
         unsigned char RDRF:1;
         unsigned char ORER:1;
         unsigned char FER:1;
         unsigned char PER:1;
         unsigned char TEND:1;
         unsigned char :2;
      } BIT;
      struct {
         unsigned char TDRE:1;
         unsigned char RDRF:1;
         unsigned char ORER:1;
         unsigned char ERS:1;
         unsigned char PER:1;
         unsigned char TEND:1;
         unsigned char :2;
      } BIT2;
   } SSR;
   unsigned char RDR;
・・・
```

Furthermore, struct st_sci1, struct st_sci2, struct st_sci3, struct st_sci4, struct st_sci5, and struct st_sci6 are also in the similar manner. Therefore, modify these structures as shown above and use them.