RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A015A/E	Rev.	1.00
Title	RL78/L12 Direction of use		Information Category	Technical Notification		
Applicable Product	RL78/L12 Group R5F10RxxA, R5F10RxxG Please see Appendix1.	Lot No.	Reference Document	RL78/L12 User's Manual: Hardware Rev. 1.00 R01UH0330EJ0100 (Jan. 2013)		
		All lot				

"Operating Precaution for Data Flash read access" directions of use on these products have been added to "RL78/L12".

1. Restriction:

Applicable Usage:

The usage which meets to all of (1), (2), and (3) is applicable to the restriction.

(1) Using both DMA and Data Flash.

(2) DMA is operating when Data Flash [Note1] read occurs.

(3) Data Flash is read using flash-related libraries Renesas Electronics is offering, which are listed below. Otherwise instead of using those libraries, the combination of CPU Related instructions [Note2] are used for reading related memory [Note3] and Data Flash.

- The EEL(EEPROM emulation library) [Note1] Pack01 V1.12 or earlier version.
- The FDL(Data Flash library) Type01 V1.11 or earlier version.
- The FDL Type02 V1.00 or earlier version.
- The FDL Type04 V1.04 or earlier version.

Note1. When EEL is used, commands other than READ command are also related: they also make read access to the Data Flash.

Note2. See Appendix2 about the combination of the related instructions1 and 2.

Note3. Related memory is RAM(Include general purpose register area),SFR,2nd SFR,ES,CS,PSW,SP

Detail of Restriction:

In the case that DMA transfer is operated and it is immediately followed by read access to the target memory (Related instructions 1) which access is also immediately followed in sequence, by read access to Data Flash (Related instructions 2), because of the conflict on the internal bus between read access to the target memory and to the Data Flash, the read out result from the target memory may be wrongly changed.

```
Example for an instruction sequence causing this issue:


    DMA transfer trigger
    DMA transfer
MOVW        HL,!addr16      ; read data from RAM (Related instruction 1)
MOV         A,[DE]          ; read data from Data Flash (Related instructions 2)

When DMA transfer occurs as mentioned above timing, a wrong data is loaded into HL register.
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2. Workaround

If you have any possibility that read access to the Data Flash and the DMA transfer could operate in the same time, please apply the following procedures according to the way to read out the Data Flash.

Case 1:

Data Flash Read access via the 'Data Flash Access Library' (FDL) and/or EEPROM Emulation Library (EEL). Both libraries are developed under the responsibility of Renesas.

Workaround for Case 1:

There are currently one type of EEL supported and three type of FDL supported and all of them will be updated to cover the aforementioned workaround.

Library version (Not installer version)

EEL (Pack01) version V1.13 [Note] or later

FDL (Type01) version V1.12 [Note] or later

FDL (Type02) version V1.01 [Note] or later

FDL (Type04) version V1.05 [Note] or later

Case 2:

Data Flash Read access directly executed in the user software without library.

Workaround for Case 2:

Please apply either of the following procedures.

(A) Holding DMA or forcing termination DMA

In case, the user software has to perform a direct Data Flash Read access without using the FDL read commend, any possible DMA transfer must be stopped before the Data Flash read access is executed. To stop any DMA transfer, please follow the procedure given in the User Manual.

Furthermore, please make sure to wait at least 3 clocks(f_{CLK}) after setting DWAITn bit to "1" before the Data Flash read instruction is executed. Restart any DMA transfer (by clearing DWAITn bit to "0") after the Data Flash read access have been finished.

(B) Reading Data Flash by using library

When access Data Flash, please use latest Data Flash library of case 1.

(C) Inserting a NOP instruction

Such kind of conflict can be avoided by inserting a NOP instruction immediately prior to any Data Flash Read access.

Example to avoid this issue: operand

```
MOVW    HL, !addr16    ; Read data from RAM
NOP                    ; Insert a NOP prior to the DF read access
MOV     A,[DE]         ; Read data from Data Flash
```

In case the application software will use the DMA feature, Renesas strongly recommend not to perform a direct Data Flash Read access in the user software, because in case of a high level language (e.g. C-Language) it cannot be avoided that the C-compiler may generate a code sequence as described before. Therefore, Renesas strongly recommend to perform the Data Flash Read access ONLY via the corresponding FDL read command.

Note. The modified version of EEL(EEPROM Emulation library) and FDL(Data Flash library) will be released in sequence after July 2013.

Remark. f_{CLK}: CPU/peripheral hardware clock frequency

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3. Modification schedule

  This matter is added to "Procedure for accessing data flash memory" of CHAPTER 26 FLASH MEMORY in the user's manual by the next revision.

4. List of usage restrictions

No.	Description	Products
		RL78/L12 Group R5F10RxxA, R5F10RxxG (Please see Appendix1.)
1	Operating Precaution for Data Flash read access	X

Remark The meaning of each symbol is as follows:

    X: Restriction applicable

    -: Restriction not applicable

5. Revision history

Revision history of RL78/L12 directions of use

Document Number	Issued Date	Description
TN-RL*-A015A/E	Aug. 19, 2013	First edition issued List of usage restriction: No.1 (This document)

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Appendix1

[Target products' name list]

RL78/L12 (R5F10R)

32-pin LQFP 7x7mm	R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP, R5F10RB8GFP, R5F10RBAGFP, R5F10RBCGFP
44-pin LQFP 10x10mm	R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP, R5F10RF8GFP, R5F10RFAGFP, R5F10RFCGFP
48-pin LFQFP 7x7mm	R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB, R5F10RG8GFB, R5F10RGAGFB, R5F10RGCGFB
52-pin LQFP 10x10mm	R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA, R5F10RJ8GFA, R5F10RJAAGA, R5F10RJCGFA
64-pin WQFN 8x8mm	R5F10RLAANB, R5F10RLCANB, R5F10RLAGNB, R5F10RLCGNB
64-pin LFQFP 10x10mm	R5F10RLAAFB, R5F10RLCAFB, R5F10RLAGFB, R5F10RLCGFB
64-pin LQFP 12x12mm	R5F10RLAAFA, R5F10RLCAFA, R5F10RLAGFA, R5F10RLCGFA

Appendix2-1

[Related instructions list]

In case that the Data Flash is read out by "Related instructions 2" immediately after the target memory is read out by "Related instructions 1", this is within the restriction; however, particular combinations of related instructions shown in Appendix2-2 are excepted.

Related instructions 1: Read instructions of RAM(Include general purpose register area), SFR,2nd SFR,ES,CS, PSW,SP
Note: Read instructions of mirror area and Data Flash are not related.

	Operand			Operand			Operand			Operand			Operand
MOV	A, saddr		ADDC	A, saddr		XOR	A, saddr		MOV	ES, saddr		MOV1	CY, saddr.bit
	A, sfr			A, !addr16			A, !addr16			B, saddr			CY, sfr.bit
	A, !addr16			A, [HL]			A, [HL]			B, !addr16			CY, PSW.bit
	A, PSW			A, [HL+byte]			A, [HL+byte]			C, saddr			CY, [HL].bit
	A, ES			A, [HL+B]			A, [HL+B]			C, !addr16		AND1	CY, saddr.bit
	A, CS			A, [HL+C]			A, [HL+C]			X, saddr			CY, sfr.bit
	A, [DE]		SUB	A, saddr		CMP	A, saddr			X, !addr16			CY, PSW.bit
	A, [DE+byte]			A, !addr16			A, !addr16		MOVW	BC, saddrp			CY, [HL].bit
	A, [HL]			A, [HL]			A, [HL]			BC, !addr16		OR1	CY, saddr.bit
	A, [HL+byte]			A, [HL+byte]			A, [HL+byte]			DE, saddrp			CY, sfr.bit
	A, [HL+B]			A, [HL+B]			A, [HL+B]			DE, !addr16			CY, PSW.bit
	A, [HL+C]			A, [HL+C]			A, [HL+C]			HL, saddrp			CY, [HL].bit
	A, word[B]		SUBC	A, saddr		ADDW	AX, saddrp			HL, !addr16		XOR1	CY, saddr.bit
	A, word[C]			A, !addr16			AX, !addr16			BC, SP			CY, sfr.bit
	A, word[BC]			A, [HL]			AX, [HL+byte]			DE, SP			CY, PSW.bit
	A, [SP+byte]			A, [HL+byte]		SUBW	AX, saddrp			HL, SP			CY, [HL].bit
MOVW	AX, saddrp			A, [HL+B]			AX, !addr16		CMP	saddr, #byte		POP	rp
	AX, sfrp			A, [HL+C]			AX, [HL+byte]			!addr16, #byte			
	AX, !addr16		AND	A, saddr		CMPW	AX, saddrp		CMP0	saddr			
	AX, [DE]			A, !addr16			AX, !addr16			!addr16			
	AX, [DE+byte]			A, [HL]			AX, [HL+byte]		CMPS	X, [HL+byte]			
	AX, [HL]			A, [HL+byte]		MOVW	AX, SP						
	AX, [HL+byte]			A, [HL+B]									
	AX, word[B]			A, [HL+C]									
	AX, word[C]		OR	A, saddr									
	AX, word[BC]			A, !addr16									
	AX, [SP+byte]			A, [HL]									
ADD	A, saddr			A, [HL+byte]									
	A, !addr16			A, [HL+B]									
	A, [HL]			A, [HL+C]									
	A, [HL+byte]												
	A, [HL+B]												
	A, [HL+C]												

Related instructions 2: Read instructions of Data Flash

	Operand			Operand			Operand			Operand
MOV	A, !addr16		ADD	A, !addr16		AND	A, !addr16		MOV	B, !addr16
	A, [DE]			A, [HL]			A, [HL]			C, !addr16
	A, [DE+byte]			A, [HL+byte]			A, [HL+byte]			X, !addr16
	A, [HL]			A, [HL+B]			A, [HL+B]		CMP	!addr16, #byte
	A, [HL+byte]			A, [HL+C]			A, [HL+C]		CMP0	!addr16
	A, [HL+B]		ADDC	A, !addr16		OR	A, !addr16		CMPS	X, [HL+byte]
	A, [HL+C]			A, [HL]			A, [HL]			
	A, word[B]			A, [HL+byte]			A, [HL+byte]			
	A, word[C]			A, [HL+B]			A, [HL+B]			
	A, word[BC]			A, [HL+C]			A, [HL+C]			
			SUB	A, !addr16		XOR	A, !addr16			
				A, [HL]			A, [HL]			
				A, [HL+byte]			A, [HL+byte]			
				A, [HL+B]			A, [HL+B]			
				A, [HL+C]			A, [HL+C]			
			SUBC	A, !addr16		CMP	A, !addr16			
				A, [HL]			A, [HL]			
				A, [HL+byte]			A, [HL+byte]			
				A, [HL+B]			A, [HL+B]			
				A, [HL+C]			A, [HL+C]			

Appendix2-2

Safe combinations of related instructions1 and 2 <1>

Related instruction 1		Related instruction 2	
	Operand		**Operand**
MOVW	DE, saddrp	MOV	A, [DE]
	DE, !addr16		A, [DE+byte]
	DE, SP		
POP	DE		

Safe combinations of related instructions1 and 2 <2>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOVW	HL, saddrp	MOV	A, [HL]	ADD	A, [HL]	AND	A, [HL]
	HL, !addr16		A, [HL+byte]		A, [HL+byte]		A, [HL+byte]
	HL, SP		A, [HL+B]		A, [HL+B]		A, [HL+B]
POP	HL		A, [HL+C]		A, [HL+C]		A, [HL+C]
				ADDC	A, [HL]	OR	A, [HL]
			Operand		A, [HL+byte]		A, [HL+byte]
		CMPS	X, [HL+byte]		A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]
				SUB	A, [HL]	XOR	A, [HL]
					A, [HL+byte]		A, [HL+byte]
					A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]
				SUBC	A, [HL]	CMP	A, [HL]
					A, [HL+byte]		A, [HL+byte]
					A, [HL+B]		A, [HL+B]
					A, [HL+C]		A, [HL+C]

Safe combinations of related instructions1 and 2 <3>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOV	B, saddr	MOV	A, [HL+B]	ADD	A, [HL+B]	AND	A, [HL+B]
	B, !addr16		A, word[B]	ADDC	A, [HL+B]	OR	A, [HL+B]
MOVW	BC, saddrp			SUB	A, [HL+B]	XOR	A, [HL+B]
	BC, !addr16			SUBC	A, [HL+B]	CMP	A, [HL+B]
	BC, SP						
POP	BC						

Safe combinations of related instructions1 and 2 <4>

Related instruction 1		Related instruction 2					
	Operand		**Operand**		**Operand**		**Operand**
MOV	C, saddr	MOV	A, [HL+C]	ADD	A, [HL+C]	AND	A, [HL+C]
	C, !addr16		A, word[C]	ADDC	A, [HL+C]	OR	A, [HL+C]
MOVW	BC, saddrp			SUB	A, [HL+C]	XOR	A, [HL+C]
	BC, !addr16			SUBC	A, [HL+C]	CMP	A, [HL+C]
	BC, SP						
POP	BC						

Safe combinations of related instructions1 and 2 <5>

Related instruction 1		Related instruction 2	
	Operand		**Operand**
MOV	B, saddr	MOV	A, word[BC]
	B, !addr16		
	C, saddr		
	C, !addr16		
MOVW	BC, saddrp		
	BC, !addr16		
	BC, SP		
POP	BC		