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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0122A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/H1D Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/H1D Group	Lot No. All lots	Reference Document	RL78/H1D User's Manual: Hardware Rev. 1.00 R01UH0756EJ0100 (Apr. 2022)		

This document describes misstatements found in the RL78/H1D User's Manual: Hardware Rev. 1.00 (R01UH0756EJ0100).

Corrections

Applicable Item	Applicable Page	Contents
8.3.4 Real-time clock control register 1 (RTCC1)	Page 344	Incorrect descriptions revised
Figure 8 - 21. Procedure for Reading Real-time Clock 2	Page 358	Incorrect descriptions revised
Figure 8 - 22. Procedure for Writing Real-time Clock 2	Page 359	Incorrect descriptions revised
38.3.2 Supply current characteristics	Page 1158 to Page 1160	Incorrect descriptions revised
39.3.2 Supply current characteristics	Page 1219 to Page 1222	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0756EJ0100	
1	8.3.4 Real-time clock control register 1 (RTCC1)		Page 344	Page 3
2	Figure 8 - 21 Procedure for Reading Real-time Clock 2		Page 358	Page 4
3	Figure 8 - 22 Procedure for Writing Real-time Clock 2		Page 359	Page 4
4	38.3.2 Supply current characteristics		Page 1158 to Page 1160	Page 5 to Page 7
5	39.3.2 Supply current characteristics		Page 1219 to Page1222	Page 8 to Page 10

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/H1D Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0122A/E	Jan. 20, 2023	First edition issued Corrections No.1 to No.5 revised (this document)

1. 8.3.4 Real-time clock control register 1 (RTCC1) (Page 344)

Incorrect:

Figure 8 - 7. Format of Real-time Clock Control Register 1 (RTCC1) (3/3)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	RITE	WAFG	RIFG	0	RWST	RWAIT

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value

This status flag indicates whether the setting of the RWAIT bit is valid.

Before reading or writing the counter value, confirm that the value of this flag is 1.

Even if the RWAIT bit is set to 0, the RWST bit is not set to 0 while writing to the counter. After writing is completed, the RWST bit is set to 0.

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.

Be sure to write “1” to it to read or write the counter value.

As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.

When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1).[Notes 1, 2]

When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.

However, when it wrote a value to second count register, it will not keep the overflow event.

Correct:

Figure 8 - 7. Format of Real-time Clock Control Register 1 (RTCC1) (3/3)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	RITE	WAFG	RIFG	0	RWST	RWAIT

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value

This status flag indicates whether the setting of the RWAIT bit is valid.

Before reading or writing the counter value, confirm that the value of this flag is 1.

Even if the RWAIT bit is set to 0, the RWST bit is not set to 0 while writing to the counter. After writing is completed, the RWST bit is set to 0.

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.

Be sure to write “1” to it to read or write the counter value.

As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).

Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.

When RWAIT = 1, it takes up to one cycle of f_{RTC} until the counter value can be read or written (RWST = 1).[Notes 1, 2]

When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.

However, when it wrote a value to second count register, it will not keep the overflow event.

2. Figure 8 - 21. Procedure for Reading Real-time Clock (Page 358)

Incorrect:

Note 1. When the counter is stopped (RTCE = 0), RWST is not set to 1.

Note 2. Be sure to confirm that RWST = 0 before setting **STOP** mode.

Caution **Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence. All the registers do not have to be set and only some registers may be read.

Correct:

Note 1. When the counter is stopped (RTCE = 0), RWST is not set to 1.

Note 2. Be sure to confirm that RWST = 0 before setting **HALT/STOP** mode.

Caution **Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence. All the registers do not have to be set and only some registers may be read.

3. Figure 8 - 22. Procedure for Writing Real-time Clock (Page 359)

Incorrect:

Note 1. When the counter is stopped (RTCE = 0), RWST is not set to 1.

Note 2. Be sure to confirm that RWST = 0 before setting **STOP** mode.

Cautions 1. **Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.**

Cautions 2. **When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence. All the registers do not have to be set and only some registers may be written.

Correct:

Note 1. When the counter is stopped (RTCE = 0), RWST is not set to 1.

Note 2. Be sure to confirm that RWST = 0 before setting **HALT/STOP** mode.

Cautions 1. **Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

Cautions 2. **When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.**

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be read in any sequence. All the registers do not have to be set and only some registers may be written.

4. 38.3.2 Supply current characteristics (Page 1158 to Page 1160)

Incorrect:

38.3.2 Supply current characteristics

(TA = -40 to +85° C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) (1/2)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 6	IDD1	Operating mode	HS (high-speed main) mode Note 5	fIH = 24 MHz Note 3	Basic operation	VDD = 5.0 V			1.7		mA
						VDD = 3.0 V			1.7		
					Normal operation	VDD = 5.0 V			3.7	6.2	
						VDD = 3.0 V			3.7	6.2	
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input			4.7	9.2	
						Resonator connection			5.1	9.2	
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input			5.2	12.6	
						Resonator connection			5.7	12.6	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.** The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the real-time clock 2, 12-bit interval timer, and watchdog timer.**

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 6. I_{DD1} do not include the current flowing to the AFE.
The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency.

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Correct:

38.3.2 Supply current characteristics

(TA = -40 to +85° C, 2.4 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) (1/2)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 6	IDD1	Operating mode	HS (high-speed main) mode Note 5	fIH = 24 MHz Note 3	Basic operation	VDD = 5.0 V			1.7		mA
						VDD = 3.0 V			1.7		
					Normal operation	VDD = 5.0 V			3.7	6.2	
						VDD = 3.0 V			3.7	6.2	
				fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input			4.7	9.2	
						Resonator connection			5.1	9.2	
				fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input			5.2	12.6	
						Resonator connection			5.7	12.6	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main) mode.
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2. The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 6. I_{DD1} do not include the current flowing to the AFE.
The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency.

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = -40 to +85° C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 9	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	1.83	mA
					V_{DD} = 3.0 V		0.42	1.83	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.38	
					V_{DD} = 3.0 V		0.39	1.38	
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.26	1.55	mA
					Resonator connection		0.40	1.68	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.25	1.55	
					Resonator connection		0.40	1.68	
				f_{MX} = 16 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.23	1.22	
					Resonator connection		0.36	1.39	
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.22	1.22	
					Resonator connection		0.35	1.39	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.82	
					Resonator connection		0.29	0.90	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.18	0.82	
					Resonator connection		0.28	0.90	
	I_{DD3} Note 6	STOP mode Note 8	T_A = -40°C				0.20	0.59	μA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.** The current flowing into AFE is not included.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the real-time clock 2 is included. However, not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.**

Note 6. **Not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.**

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

(TA = -40 to +85° C, 2.4 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Notes 1, Note 8	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	1.83	mA
					V_{DD} = 3.0 V		0.42	1.83	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.38	
					V_{DD} = 3.0 V		0.39	1.38	
			HS (high-speed main) mode Note 6	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.26	1.55	mA
					Resonator connection		0.40	1.68	
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.25	1.55	
					Resonator connection		0.40	1.68	
				f_{MX} = 16 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.23	1.22	
					Resonator connection		0.36	1.39	
				f_{MX} = 16 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.22	1.22	
					Resonator connection		0.35	1.39	
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.82	
					Resonator connection		0.29	0.90	
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.18	0.82	
					Resonator connection		0.28	0.90	
	I_{DD3}	STOP mode Note 8	T_A = -40°C				0.20	0.59	μA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main) mode.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time clock 2.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. The current flowing into AFE is not included.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

Note 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Note 7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Note 9. I_{DD2} and I_{DD3} do not include the current flowing to the AFE.
The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Note 8. I_{DD2} and I_{DD3} do not include the current flowing to the AFE.
The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and AFE current (AV_{DD} systems) when the AFE operates in the operating mode, HALT mode, or STOP mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

5. 39.3.2 Supply current characteristics (Page 1219 to Page1222)

Incorrect:

39.3.2 Supply current characteristics

(TA = -40 to +85° C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) (1/2)

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) Mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V			1.7		mA
						V_{DD} = 3.0 V			1.7		
					Normal operation	V_{DD} = 5.0 V			3.7	6.4	
						V_{DD} = 3.0 V			3.7	6.4	
				f_{SUB} = 38.4 kHz Note 4 T_A = +70°C	Normal operation	Square wave input			5.5	10.8	
						Resonator connection			6.0	10.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +85°C	Normal operation	Square wave input			6.1	14.8	
						Resonator connection			6.7	14.8	

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.** The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the real-time clock 2, 12-bit interval timer, and watchdog timer.**

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency.

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition for the TYP. value is T_A = 25°C.

Correct:

39.3.2 Supply current characteristics

(TA = -40 to +85° C, 1.8 V ≤ AVDD = VDD ≤ 5.5 V, AVSS = VSS = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) Mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		
					Normal operation	V_{DD} = 5.0 V		3.7	6.4	
						V_{DD} = 3.0 V		3.7	6.4	
				f_{SUB} = 38.4 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.5	10.8	
						Resonator connection		6.0	10.8	
				f_{SUB} = 38.4 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.1	14.8	
						Resonator connection		6.7	14.8	

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), and LS (low-speed main) modes.
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time Clock 2. The current flowing into AFE is not included.

Note 2. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 3. When high-speed system clock and subsystem clock are stopped.

Note 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

Note 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency.

Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 4. Except subsystem clock operation, temperature condition for the TYP. value is T_A = 25°C.

(TA = -40 to +85° C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) Mode ~~Note 7~~	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	2.03	mA
					V_{DD} = 3.0 V		0.42	2.03	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.58	
					V_{DD} = 3.0 V		0.39	1.58	
			LS (low-speed main) Mode ~~Note 7~~	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		0.25	0.81	mA
					V_{DD} = 2.0 V		0.25	0.81	
			HS (high-speed main) Mode ~~Note 7~~	f_{MX} = 20 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.26	1.75	mA
					Resonator connection		0.40	1.88	
				f_{MX} = 20 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.25	1.75	
					Resonator connection		0.40	1.88	
				f_{MX} = 16 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.23	1.42	
					Resonator connection		0.36	1.59	
				f_{MX} = 16 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.22	1.42	
					Resonator connection		0.35	1.59	
				f_{MX} = 10 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.19	0.92	
					Resonator connection		0.29	1.00	
				f_{MX} = 10 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.18	0.92	
					Resonator connection		0.28	1.00	
			LS (low-speed main) Mode ~~Note 7~~	f_{MX} = 8 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.09	0.61	mA
					Resonator connection		0.15	0.66	
				f_{MX} = 8 MHz Note 3 V_{DD} = 2.0 V	Square wave input		0.10	0.62	
					Resonator connection		0.15	0.67	
	I_{DD3} ~~Note 6~~	STOP mode ~~Note 8~~	T_A = -40°C				0.20	0.59	µA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.** The current flowing into AFE is not included.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the real-time clock 2 is included. However, not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.**

(TA = -40 to +85° C, 1.8 V ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) Mode Note 6	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.42	2.03	mA
					V_{DD} = 3.0 V		0.42	2.03	
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.39	1.58	
					V_{DD} = 3.0 V		0.39	1.58	
			LS (low-speed main) Mode Note 6	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		0.25	0.81	mA
					V_{DD} = 2.0 V		0.25	0.81	
			HS (high-speed main) Mode Note 6	f_{MX} = 20 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.26	1.75	mA
					Resonator connection		0.40	1.88	
				f_{MX} = 20 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.25	1.75	
					Resonator connection		0.40	1.88	
				f_{MX} = 16 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.23	1.42	
					Resonator connection		0.36	1.59	
				f_{MX} = 16 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.22	1.42	
					Resonator connection		0.35	1.59	
				f_{MX} = 10 MHz Note 3 V_{DD} = 5.0 V	Square wave input		0.19	0.92	
					Resonator connection		0.29	1.00	
				f_{MX} = 10 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.18	0.92	
					Resonator connection		0.28	1.00	
			LS (low-speed main) Mode Note 6	f_{MX} = 8 MHz Note 3 V_{DD} = 3.0 V	Square wave input		0.09	0.61	mA
					Resonator connection		0.15	0.66	
				f_{MX} = 8 MHz Note 3 V_{DD} = 2.0 V	Square wave input		0.10	0.62	
					Resonator connection		0.15	0.67	
	I_{DD3}	STOP mode Note 7	T_A = -40°C				0.20	0.59	µA
			T_A = +25°C				0.26	0.72	
			T_A = +50°C				0.33	1.30	
			T_A = +70°C				0.53	2.60	
			T_A = +85°C				0.93	4.85	

Note 1. Total current flowing into V_{DD} and AV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), and LS (low-speed main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the real-time Clock 2.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. The current flowing into AFE is not included.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator and subsystem clock are stopped.

Note 4. When high-speed system clock and subsystem clock are stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

Note 6. Not including the current flowing into the 12-bit interval timer, 8-bit interval timer, and watchdog timer.

Note 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Note 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

Note 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @ 1 MHz to 8 MHz

Note 7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
Remark 2. f_{IH}: High-speed on-chip oscillator clock frequency
Remark 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
Remark 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.