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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-RL*-A0152A/E	Rev.	1.00
Title	RL78/G24 Group Limitations when using the comparator		Information Category	Technical Notification		
Applicable Product	RL78/G24 Group	Lot No. All	Reference Document	RL78/G24 Group User's Manual: Hardware Rev.1.20 (R01UH0961EJ0120)		

Regarding the comparator installed in the above product, there are the following restrictions:

Restrictions

If the analog input voltage or reference input voltage of the comparator changes rapidly with a slope exceeding ±3.0 V/μs, or if the DAC output used as the reference input voltage has a change range exceeding 1V or a change interval less than 1μs, a pulse with a width of up to 150 ns may appear in the result of comparison.

Countermeasures

If the pulse appearing in the comparison result causes problems, please implement the following countermeasures:

- Set the CiFCK[1:0] bits (i = 0 - 3) to enable the digital filter (3-time match) so that noise of up to 150ns can be removed.
- In polling of the CiMON flag (i=0 - 3), ensure that short pulses can be eliminated by setting the polling interval to at least 150 ns.