

# RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0104A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G13 Descriptions in the User's Manual: Hardware Rev. 3.51 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G13 Group	Lot No.	Reference Document	RL78/G13 User's Manual: Hardware Rev. 3.51 R01UH0146EJ0351 (Dec. 2022)		
		All lots				

This document describes misstatements found in the RL78/G13 User's Manual: Hardware Rev. 3.51 (R01UH0146EJ0351).

## Corrections

Applicable Item	Applicable Page	Contents
7.3.4 Real-time clock control register 1 (RTCC1)	Page 383	Incorrect descriptions revised
Figure 7-21. Procedure for Reading Real-time Clock	Page 395	Incorrect descriptions revised
Figure 7-22. Procedure for Writing Real-time Clock	Page 396	Incorrect descriptions revised
29.3.2 Supply current characteristics	Page 938 to Page 949	Incorrect descriptions revised
30.3.2 Supply current characteristics	Page 1007 to Page 1014	Incorrect descriptions revised

## Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0146EJ0351	
1	7.3.4 Real-time clock control register 1 (RTCC1)		Page 383	Page 3
2	Figure 7-21. Procedure for Reading Real-time Clock		Page 395	Page 4
3	Figure 7-22. Procedure for Writing Real-time Clock		Page 396	Page 4
4	29.3.2 Supply current characteristics		Page 938 to Page 949	Page 5 to Page 13
5	30.3.2 Supply current characteristics		Page 1007 to Page 1014	Page 14 to Page 19

**Incorrect**; **Bold with underline**; Correct: Gray hatched

**Revision History**

RL78/G13 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0104A/E	Jan. 19, 2023	First edition issued Corrections No.1 to No.5 revised (this document)

1. **7.3.4 Real-time clock control register 1 (RTCC1) (Page 383)**

Incorrect:

Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.

This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to "1".  
This flag is cleared when "0" is written to it. Writing "1" to it is invalid.

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value

This status flag indicates whether the setting of the RWAIT bit is valid.  
Before reading or writing the counter value, confirm that the value of this flag is 1.

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.  
Be sure to write "1" to it to read or write the counter value.  
As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0.  
When RWAIT = 1, it takes up to one cycle of  $f_{RTC}$  until the counter value can be read or written (RWST = 1).<sup>Notes 1, 2</sup> When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.  
However, when it wrote a value to second count register, it will not keep the overflow event.

Correct:

Figure 7-5. Format of Real-time Clock Control Register 1 (RTCC1) (2/2)

RIFG	Constant-period interrupt status flag
0	Constant-period interrupt is not generated.
1	Constant-period interrupt is generated.

This flag indicates the status of generation of the constant-period interrupt. When the constant-period interrupt is generated, it is set to "1".  
This flag is cleared when "0" is written to it. Writing "1" to it is invalid.

RWST	Wait status flag of real-time clock
0	Counter is operating.
1	Mode to read or write counter value

This status flag indicates whether the setting of the RWAIT bit is valid.  
Before reading or writing the counter value, confirm that the value of this flag is 1.

RWAIT	Wait control of real-time clock
0	Sets counter operation.
1	Stops SEC to YEAR counters. Mode to read or write counter value

This bit controls the operation of the counter.  
Be sure to write "1" to it to read or write the counter value.  
As the internal counter (16-bit) is continuing to run, complete reading or writing within one second and turn back to 0. When reading or writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second).  
Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.  
When RWAIT = 1, it takes up to one cycle of  $f_{RTC}$  until the counter value can be read or written (RWST = 1).<sup>Notes 1, 2</sup> When the internal counter (16-bit) overflowed while RWAIT = 1, it keeps the event of overflow until RWAIT = 0, then counts up.  
However, when it wrote a value to second count register, it will not keep the overflow event.

## 2. Figure 7-21. Procedure for Reading Real-time Clock (Page 395)

### Incorrect:

**Note** Be sure to confirm that RWST = 0 before setting STOP mode.

**Caution** Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

## 3. Figure 7-22. Procedure for Writing Real-time Clock (Page 396)

### Incorrect:

**Note** Be sure to confirm that RWST = 0 before setting STOP mode.

**Cautions** 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

### Correct:

**Note** Be sure to confirm that RWST = 0 before setting STOP mode.

**Caution** Complete the series of process of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. **When reading to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be read in any sequence. All the registers do not have to read and only some registers may be read.

### Correct:

**Note** Be sure to confirm that RWST = 0 before setting STOP mode.

**Cautions** 1. Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second. **When writing to the counter is required while generation of the alarm interrupt is enabled, first set the CT2 to CT0 bits to 010B (generating the constant-period interrupt once per 1 second). Then, complete the processing from setting the RWAIT bit to 1 to setting it to 0 before generation of the next constant-period interrupt.**

2. When changing the values of the SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR register while the counter operates (RTCE = 1), rewrite the values of the MIN register after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG, RIFG and RTCIF flags after rewriting the MIN register.

**Remark** The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence. All the registers do not have to be set and only some registers may be written.

4. **29.3.2 Supply current characteristics (Page 938 to Page 949)**

Incorrect:

**29.3.2 Supply current characteristics**

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**

**(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (1/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>HI</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V		2.1		mA
						V <sub>DD</sub> = 3.0 V		2.1		mA
					Normal operation	V <sub>DD</sub> = 5.0 V		4.6	7.0	mA
						V <sub>DD</sub> = 3.0 V		4.6	7.0	mA
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input		4.6	7.7	μA
				T <sub>A</sub> = +85°C		Resonator connection		4.7	7.8	μA

**Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>HI</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

Correct:

**29.3.2 Supply current characteristics**

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**

**(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (1/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>HI</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V		2.1		mA
						V <sub>DD</sub> = 3.0 V		2.1		mA
					Normal operation	V <sub>DD</sub> = 5.0 V		4.6	7.0	mA
						V <sub>DD</sub> = 3.0 V		4.6	7.0	mA
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input		4.6	7.7	μA
				T <sub>A</sub> = +85°C		Resonator connection		4.7	7.8	μA

**Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>HI</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 2	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.54	1.63	mA	
					V <sub>DD</sub> = 3.0 V		0.54	1.63	mA	
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.44	1.28	mA	
					V <sub>DD</sub> = 3.0 V		0.44	1.28	mA	
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.40	1.00	mA	
					V <sub>DD</sub> = 3.0 V		0.40	1.00	mA	
				LS (low-speed main) mode Note 2	f <sub>IH</sub> = 8 MHz Note 4	V <sub>DD</sub> = 3.0 V		260	530	μA
					V <sub>DD</sub> = 2.0 V		260	530	μA	
				LV (low-voltage main) mode Note 2	f <sub>IH</sub> = 4 MHz Note 4	V <sub>DD</sub> = 3.0 V		420	640	μA
						V <sub>DD</sub> = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 2	f <sub>MX</sub> = 20 MHz Note 3	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				V <sub>DD</sub> = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f <sub>MX</sub> = 20 MHz Note 3	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				V <sub>DD</sub> = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			f <sub>MX</sub> = 10 MHz Note 3	Square wave input		0.19	0.60	mA		
				Resonator connection		0.26	0.67	mA		
LS (low-speed main) mode Note 2	f <sub>MX</sub> = 8 MHz Note 3	Square wave input		95	330	μA				
		Resonator connection		145	380	μA				
	V <sub>DD</sub> = 3.0 V	Square wave input		95	330	μA				
		Resonator connection		145	380	μA				
f <sub>MX</sub> = 8 MHz Note 3	Square wave input		95	330	μA					
	Resonator connection		145	380	μA					
V <sub>DD</sub> = 2.0 V	Square wave input		95	330	μA					
	Resonator connection		145	380	μA					

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
I <sub>DD3</sub> Note 5	STOP mode Note 5	T <sub>A</sub> = -40°C				0.18	0.50	μA	
						0.23	0.50	μA	
						0.30	1.10	μA	
						0.46	1.90	μA	
						0.75	3.30	μA	

- Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 6	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.54	1.63	mA	
					V <sub>DD</sub> = 3.0 V		0.54	1.63	mA	
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.44	1.28	mA	
					V <sub>DD</sub> = 3.0 V		0.44	1.28	mA	
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.40	1.00	mA	
					V <sub>DD</sub> = 3.0 V		0.40	1.00	mA	
				LS (low-speed main) mode Note 6	f <sub>IH</sub> = 8 MHz Note 4	V <sub>DD</sub> = 3.0 V		260	530	μA
					V <sub>DD</sub> = 2.0 V		260	530	μA	
				LV (low-voltage main) mode Note 6	f <sub>IH</sub> = 4 MHz Note 4	V <sub>DD</sub> = 3.0 V		420	640	μA
						V <sub>DD</sub> = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 6	f <sub>MX</sub> = 20 MHz Note 3	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				V <sub>DD</sub> = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				f <sub>MX</sub> = 20 MHz Note 3	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
				V <sub>DD</sub> = 3.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
			f <sub>MX</sub> = 10 MHz Note 3	Square wave input		0.19	0.60	mA		
				Resonator connection		0.26	0.67	mA		
LS (low-speed main) mode Note 6	f <sub>MX</sub> = 8 MHz Note 3	Square wave input		95	330	μA				
		Resonator connection		145	380	μA				
	V <sub>DD</sub> = 3.0 V	Square wave input		95	330	μA				
		Resonator connection		145	380	μA				
f <sub>MX</sub> = 8 MHz Note 3	Square wave input		95	330	μA					
	Resonator connection		145	380	μA					
V <sub>DD</sub> = 2.0 V	Square wave input		95	330	μA					
	Resonator connection		145	380	μA					

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
I <sub>DD3</sub> Note 7	STOP mode Note 7	T <sub>A</sub> = -40°C				0.18	0.50	μA	
						0.23	0.50	μA	
						0.30	1.10	μA	
						0.46	1.90	μA	
						0.75	3.30	μA	

- Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
  - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). ~~The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.~~
6. ~~Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.~~
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
  - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{\infty} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
  - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
  - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator and subsystem clock are stopped.
4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
  - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{\infty} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
  - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
  - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	f <sub>IH</sub> = 32 MHz Note 3	Basic operation	V <sub>DD</sub> = 5.0 V	2.3		mA	
						V <sub>DD</sub> = 3.0 V	2.3		mA	
						Normal operation	V <sub>DD</sub> = 5.0 V	5.2	8.5	mA
							V <sub>DD</sub> = 3.0 V	5.2	8.5	mA
				f <sub>SUB</sub> = 32.768 kHz Note 4	Normal operation	Square wave input	5.7	13.3	μA	
				T <sub>A</sub> = +85°C		Resonator connection	5.8	13.4	μA	

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**
    - When high-speed on-chip oscillator and subsystem clock are stopped.
    - When high-speed system clock and subsystem clock are stopped.
    - When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
    - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
      - HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz
      - LS (low-speed main) mode: 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz
      - LV (low-voltage main) mode: 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	f <sub>IH</sub> = 32 MHz Note 3	Basic operation	V <sub>DD</sub> = 5.0 V	2.3		mA	
						V <sub>DD</sub> = 3.0 V	2.3		mA	
						Normal operation	V <sub>DD</sub> = 5.0 V	5.2	8.5	mA
							V <sub>DD</sub> = 3.0 V	5.2	8.5	mA
				f <sub>SUB</sub> = 32.768 kHz Note 4	Normal operation	Square wave input	5.7	13.3	μA	
				T <sub>A</sub> = +85°C		Resonator connection	5.8	13.4	μA	

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.**
    - The currents in the "TYP." column do not include the operating currents of the peripheral modules.
    - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

    - When high-speed on-chip oscillator and subsystem clock are stopped.
    - When high-speed system clock and subsystem clock are stopped.
    - When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
    - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
      - HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz
      - LS (low-speed main) mode: 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz
      - LV (low-voltage main) mode: 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C



(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 2	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.62	1.86	mA
					V <sub>DD</sub> = 3.0 V	0.62	1.86	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.50	1.45	mA
					V <sub>DD</sub> = 3.0 V	0.50	1.45	mA
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	1.11	mA
					V <sub>DD</sub> = 3.0 V	0.44	1.11	mA
			LS (low-speed main) mode Note 2	f <sub>IH</sub> = 8 MHz Note 4	V <sub>DD</sub> = 3.0 V	290	620	μA
				V <sub>DD</sub> = 2.0 V	290	620	μA	
			LV (low-voltage main) mode Note 2	f <sub>IH</sub> = 4 MHz Note 4	V <sub>DD</sub> = 3.0 V	440	680	μA
					V <sub>DD</sub> = 2.0 V	440	680	μA
			HS (high-speed main) mode Note 2	f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.31	1.08	mA
					V <sub>DD</sub> = 5.0 V	0.48	1.28	mA
		f <sub>MX</sub> = 20 MHz Note 3		Square wave input	0.31	1.08	mA	
				V <sub>DD</sub> = 3.0 V	0.48	1.28	mA	
		f <sub>MX</sub> = 10 MHz Note 3		Square wave input	0.21	0.63	mA	
				V <sub>DD</sub> = 5.0 V	0.28	0.71	mA	
		f <sub>MX</sub> = 10 MHz Note 3		Square wave input	0.21	0.63	mA	
				V <sub>DD</sub> = 3.0 V	0.28	0.71	mA	
		LS (low-speed main) mode Note 2		f <sub>MX</sub> = 8 MHz Note 3	Square wave input	110	360	μA
					V <sub>DD</sub> = 3.0 V	160	420	μA
f <sub>MX</sub> = 8 MHz Note 3	Square wave input		110	360	μA			
	V <sub>DD</sub> = 2.0 V		160	420	μA			

I <sub>DD3</sub>	STOP mode Note 8	T <sub>A</sub> = -40°C	0.19	0.52	μA
		T <sub>A</sub> = +25°C	0.25	0.52	μA
		T <sub>A</sub> = +50°C	0.32	2.21	μA
		T <sub>A</sub> = +70°C	0.55	3.94	μA
		T <sub>A</sub> = +85°C	1.00	7.95	μA

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
  - Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 6	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.62	1.86	mA
					V <sub>DD</sub> = 3.0 V	0.62	1.86	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.50	1.45	mA
					V <sub>DD</sub> = 3.0 V	0.50	1.45	mA
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	1.11	mA
					V <sub>DD</sub> = 3.0 V	0.44	1.11	mA
			LS (low-speed main) mode Note 6	f <sub>IH</sub> = 8 MHz Note 4	V <sub>DD</sub> = 3.0 V	290	620	μA
				V <sub>DD</sub> = 2.0 V	290	620	μA	
			LV (low-voltage main) mode Note 6	f <sub>IH</sub> = 4 MHz Note 4	V <sub>DD</sub> = 3.0 V	440	680	μA
					V <sub>DD</sub> = 2.0 V	440	680	μA
			HS (high-speed main) mode Note 6	f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.31	1.08	mA
					V <sub>DD</sub> = 5.0 V	0.48	1.28	mA
		f <sub>MX</sub> = 20 MHz Note 3		Square wave input	0.31	1.08	mA	
				V <sub>DD</sub> = 3.0 V	0.48	1.28	mA	
		f <sub>MX</sub> = 10 MHz Note 3		Square wave input	0.21	0.63	mA	
				V <sub>DD</sub> = 5.0 V	0.28	0.71	mA	
		f <sub>MX</sub> = 10 MHz Note 3		Square wave input	0.21	0.63	mA	
				V <sub>DD</sub> = 3.0 V	0.28	0.71	mA	
		LS (low-speed main) mode Note 6		f <sub>MX</sub> = 8 MHz Note 3	Square wave input	110	360	μA
					V <sub>DD</sub> = 3.0 V	160	420	μA
f <sub>MX</sub> = 8 MHz Note 3	Square wave input		110	360	μA			
	V <sub>DD</sub> = 2.0 V		160	420	μA			

I <sub>DD3</sub>	STOP mode Note 7	T <sub>A</sub> = -40°C	0.19	0.52	μA
		T <sub>A</sub> = +25°C	0.25	0.52	μA
		T <sub>A</sub> = +50°C	0.32	2.21	μA
		T <sub>A</sub> = +70°C	0.55	3.94	μA
		T <sub>A</sub> = +85°C	1.00	7.95	μA

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.**
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
  - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
- In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz

LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz

LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

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4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ).
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz

LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz

LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>ih</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V	2.6		mA	
						V <sub>DD</sub> = 3.0 V	2.6		mA	
						Normal operation	V <sub>DD</sub> = 5.0 V	6.1	9.5	mA
							V <sub>DD</sub> = 3.0 V	6.1	9.5	mA
			f <sub>sub</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input	6.6	16.3	μA		
			T <sub>A</sub> = +85°C		Resonator connection	6.7	16.4	μA		

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
  - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz  
 LS (low-speed main) mode: 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz  
 LV (low-voltage main) mode: 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>ih</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>sub</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>ih</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V	2.6		mA	
						V <sub>DD</sub> = 3.0 V	2.6		mA	
						Normal operation	V <sub>DD</sub> = 5.0 V	6.1	9.5	mA
							V <sub>DD</sub> = 3.0 V	6.1	9.5	mA
			f <sub>sub</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input	6.6	16.3	μA		
			T <sub>A</sub> = +85°C		Resonator connection	6.7	16.4	μA		

- Notes**
- Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.**
    - The currents in the "TYP." column do not include the operating currents of the peripheral modules.
    - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
  - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
 2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz  
 LS (low-speed main) mode: 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 8 MHz  
 LV (low-voltage main) mode: 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 4 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>ih</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>sub</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T<sub>A</sub> = -40 to +85° C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 2	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.62	1.89	mA
					V <sub>DD</sub> = 3.0 V	0.62	1.89	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.50	1.48	mA
					V <sub>DD</sub> = 3.0 V	0.50	1.48	mA
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	1.12	mA
					V <sub>DD</sub> = 3.0 V	0.44	1.12	mA
			LS (low-speed main) mode Note 2	f <sub>IH</sub> = 8 MHz Note 4	V <sub>DD</sub> = 3.0 V	290	620	μA
				V <sub>DD</sub> = 2.0 V	290	620	μA	
			LV (low-voltage main) mode Note 2	f <sub>IH</sub> = 4 MHz Note 4	V <sub>DD</sub> = 3.0 V	460	700	μA
					V <sub>DD</sub> = 2.0 V	460	700	μA
			HS (high-speed main) mode Note 2	f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.31	1.14	mA
					V <sub>DD</sub> = 5.0 V	0.48	1.34	mA
		Resonator connection			0.31	1.14	mA	
		V <sub>DD</sub> = 3.0 V			0.48	1.34	mA	
		f <sub>MX</sub> = 10 MHz Note 3		Square wave input	0.21	0.68	mA	
				V <sub>DD</sub> = 5.0 V	0.28	0.76	mA	
				Resonator connection	0.21	0.68	mA	
				V <sub>DD</sub> = 3.0 V	0.28	0.76	mA	
LS (low-speed main) mode Note 2	f <sub>MX</sub> = 8 MHz Note 3	Square wave input	110	390	μA			
		V <sub>DD</sub> = 3.0 V	160	450	μA			
	f <sub>MX</sub> = 8 MHz Note 3	Square wave input	110	390	μA			
		V <sub>DD</sub> = 2.0 V	160	450	μA			

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 6	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.62	1.89	mA
					V <sub>DD</sub> = 3.0 V	0.62	1.89	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.50	1.48	mA
					V <sub>DD</sub> = 3.0 V	0.50	1.48	mA
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	1.12	mA
					V <sub>DD</sub> = 3.0 V	0.44	1.12	mA
			LS (low-speed main) mode Note 6	f <sub>IH</sub> = 8 MHz Note 4	V <sub>DD</sub> = 3.0 V	290	620	μA
					V <sub>DD</sub> = 2.0 V	290	620	μA
			LV (low-voltage main) mode Note 6	f <sub>IH</sub> = 4 MHz Note 4	V <sub>DD</sub> = 3.0 V	460	700	μA
					V <sub>DD</sub> = 2.0 V	460	700	μA
			HS (high-speed main) mode Note 6	f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.31	1.14	mA
					V <sub>DD</sub> = 5.0 V	0.48	1.34	mA
		Resonator connection			0.31	1.14	mA	
		V <sub>DD</sub> = 3.0 V			0.48	1.34	mA	
		f <sub>MX</sub> = 10 MHz Note 3		Square wave input	0.21	0.68	mA	
				V <sub>DD</sub> = 5.0 V	0.28	0.76	mA	
				Resonator connection	0.21	0.68	mA	
				V <sub>DD</sub> = 3.0 V	0.28	0.76	mA	
		LS (low-speed main) mode Note 6	f <sub>MX</sub> = 8 MHz Note 3	Square wave input	110	390	μA	
				V <sub>DD</sub> = 3.0 V	160	450	μA	
			f <sub>MX</sub> = 8 MHz Note 3	Square wave input	110	390	μA	
				V <sub>DD</sub> = 2.0 V	160	450	μA	

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
STOP mode Note 8	I <sub>DD3</sub>	T <sub>A</sub> = -40°C	0.19	0.54	μA	
		T <sub>A</sub> = +25°C	0.26	0.54	μA	
		T <sub>A</sub> = +50°C	0.35	3.37	μA	
		T <sub>A</sub> = +70°C	0.68	5.98	μA	
		T <sub>A</sub> = +85°C	1.40	10.34	μA	

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
STOP mode Note 7	I <sub>DD3</sub>	T <sub>A</sub> = -40°C	0.19	0.54	μA	
		T <sub>A</sub> = +25°C	0.26	0.54	μA	
		T <sub>A</sub> = +50°C	0.35	3.37	μA	
		T <sub>A</sub> = +70°C	0.68	5.98	μA	
		T <sub>A</sub> = +85°C	1.40	10.34	μA	

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
  - Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The following points apply in the HS (high-speed main), LS (low-speed main), and LV (low-voltage main) modes.**
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
  - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
- In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz

LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz

LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

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4. When high-speed system clock and subsystem clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ).
6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz

LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz

LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

7. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

5. **30.3.2 Supply current characteristics (Page 1007 to Page 1014)**

Incorrect:

30.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
		Operating mode	HS (high-speed main) mode Note 5	f <sub>HI</sub> = 32 MHz Note 3	Basic operation					
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	f <sub>HI</sub> = 32 MHz Note 3	Basic operation	V <sub>DD</sub> = 5.0 V		2.1		mA
					V <sub>DD</sub> = 3.0 V		2.1			
		Normal operation	V <sub>DD</sub> = 5.0 V		4.6	7.5	mA			
			V <sub>DD</sub> = 3.0 V		4.6	7.5				

				f <sub>SUB</sub> = 32.768 kHz Note 4	Normal operation	Square wave input		4.6	7.7	μA	
						Resonator connection		4.7	7.8		
					T <sub>A</sub> = +85°C	Normal operation	Square wave input		6.9	19.7	μA
							Resonator connection		7.0	19.8	
				f <sub>SUB</sub> = 32.768 kHz Note 4	Normal operation	Square wave input		6.9	19.7	μA	
						Resonator connection		7.0	19.8		
				T <sub>A</sub> = +105°C	Normal operation	Square wave input		6.9	19.7	μA	
						Resonator connection		7.0	19.8		

**Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>HI</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

Correct:

30.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
		Operating mode	HS (high-speed main) mode Note 5	f <sub>HI</sub> = 32 MHz Note 3	Basic operation					
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	f <sub>HI</sub> = 32 MHz Note 3	Basic operation	V <sub>DD</sub> = 5.0 V		2.1		mA
					V <sub>DD</sub> = 3.0 V		2.1			
		Normal operation	V <sub>DD</sub> = 5.0 V		4.6	7.5	mA			
			V <sub>DD</sub> = 3.0 V		4.6	7.5				

				f <sub>SUB</sub> = 32.768 kHz Note 4	Normal operation	Square wave input		4.6	7.7	μA	
						Resonator connection		4.7	7.8		
					T <sub>A</sub> = +85°C	Normal operation	Square wave input		6.9	19.7	μA
							Resonator connection		7.0	19.8	
				f <sub>SUB</sub> = 32.768 kHz Note 4	Normal operation	Square wave input		6.9	19.7	μA	
						Resonator connection		7.0	19.8		
				T <sub>A</sub> = +105°C	Normal operation	Square wave input		6.9	19.7	μA	
						Resonator connection		7.0	19.8		

**Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. **The following points apply in the HS (high-speed main) mode.**

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>HI</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 2	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.54	2.90	mA
					V <sub>DD</sub> = 3.0 V	0.54	2.90	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	2.30	mA
					V <sub>DD</sub> = 3.0 V	0.44	2.30	mA
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.40	1.70	mA
					V <sub>DD</sub> = 3.0 V	0.40	1.70	mA
		HS (high-speed main) mode Note 2	f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.28	1.90	mA	
				Resonator connection	0.45	2.00	mA	
			f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.28	1.90	mA	
				Resonator connection	0.45	2.00	mA	
			f <sub>MX</sub> = 10 MHz Note 3	Square wave input	0.19	1.02	mA	
				Resonator connection	0.26	1.10	mA	
			f <sub>MX</sub> = 10 MHz Note 3	Square wave input	0.19	1.02	mA	
				Resonator connection	0.26	1.10	mA	

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD3</sub> Note 5	STOP mode Note 8	T <sub>A</sub> = -40°C	0.18	0.50	μA
			T <sub>A</sub> = +25°C	0.23	0.50	μA
			T <sub>A</sub> = +50°C	0.30	1.10	μA
			T <sub>A</sub> = +70°C	0.46	1.90	μA
			T <sub>A</sub> = +85°C	0.75	3.30	μA
			T <sub>A</sub> = +105°C	2.94	15.30	μA

**Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.**

- During HALT instruction execution by flash memory.
- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
- Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 6	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.54	2.90	mA
					V <sub>DD</sub> = 3.0 V	0.54	2.90	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	2.30	mA
					V <sub>DD</sub> = 3.0 V	0.44	2.30	mA
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.40	1.70	mA
					V <sub>DD</sub> = 3.0 V	0.40	1.70	mA
		HS (high-speed main) mode Note 6	f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.28	1.90	mA	
				Resonator connection	0.45	2.00	mA	
			f <sub>MX</sub> = 20 MHz Note 3	Square wave input	0.28	1.90	mA	
				Resonator connection	0.45	2.00	mA	
			f <sub>MX</sub> = 10 MHz Note 3	Square wave input	0.19	1.02	mA	
				Resonator connection	0.26	1.10	mA	
			f <sub>MX</sub> = 10 MHz Note 3	Square wave input	0.19	1.02	mA	
				Resonator connection	0.26	1.10	mA	

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD3</sub>	STOP mode Note 7	T <sub>A</sub> = -40°C	0.18	0.50	μA
			T <sub>A</sub> = +25°C	0.23	0.50	μA
			T <sub>A</sub> = +50°C	0.30	1.10	μA
			T <sub>A</sub> = +70°C	0.46	1.90	μA
			T <sub>A</sub> = +85°C	0.75	3.30	μA
			T <sub>A</sub> = +105°C	2.94	15.30	μA

**Notes 1.** Total current flowing into V<sub>DD</sub> and EV<sub>DD0</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub> or V<sub>SS</sub>, EV<sub>SS0</sub>. **The following points apply in the HS (high-speed main) mode.**

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

- During HALT instruction execution by flash memory.
- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

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6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
7. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$



(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>IH</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V	2.3		mA	
						V <sub>DD</sub> = 3.0 V	2.3			
						Normal operation	V <sub>DD</sub> = 5.0 V	5.2	9.2	mA
							V <sub>DD</sub> = 3.0 V	5.2	9.2	

				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input	5.7	13.3	μA		
						Resonator connection	5.8	13.4			
						T <sub>A</sub> = +85°C	Normal operation	Square wave input	10.0	46.0	μA
								Resonator connection	10.0	46.0	
			f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input	10.0	46.0	μA			
					Resonator connection	10.0	46.0				
			T <sub>A</sub> = +105°C			Square wave input	10.0	46.0	μA		
						Resonator connection	10.0	46.0			

**Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). **However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	f <sub>IH</sub> = 32 MHz <sup>Note 3</sup>	Basic operation	V <sub>DD</sub> = 5.0 V	2.3		mA	
						V <sub>DD</sub> = 3.0 V	2.3			
						Normal operation	V <sub>DD</sub> = 5.0 V	5.2	9.2	mA
							V <sub>DD</sub> = 3.0 V	5.2	9.2	

				f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input	5.7	13.3	μA		
						Resonator connection	5.8	13.4			
						T <sub>A</sub> = +85°C	Normal operation	Square wave input	10.0	46.0	μA
								Resonator connection	10.0	46.0	
			f <sub>SUB</sub> = 32.768 kHz <sup>Note 4</sup>	Normal operation	Square wave input	10.0	46.0	μA			
					Resonator connection	10.0	46.0				
			T <sub>A</sub> = +105°C			Square wave input	10.0	46.0	μA		
						Resonator connection	10.0	46.0			

**Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The following points apply in the HS (high-speed main) mode.**

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.

- When high-speed on-chip oscillator and subsystem clock are stopped.
- When high-speed system clock and subsystem clock are stopped.
- When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
- Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
- f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  - f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  - f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  - Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 2	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.62	3.40	mA
					V <sub>DD</sub> = 3.0 V	0.62	3.40	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.50	2.70	mA
					V <sub>DD</sub> = 3.0 V	0.50	2.70	mA
			f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	1.90	mA	
				V <sub>DD</sub> = 3.0 V	0.44	1.90	mA	
			HS (high-speed main) mode Note 2	f <sub>MX</sub> = 20 MHz Note 3, V <sub>DD</sub> = 5.0 V	Square wave input	0.31	2.10	mA
					Resonator connection	0.48	2.20	mA
		f <sub>MX</sub> = 20 MHz Note 3, V <sub>DD</sub> = 3.0 V		Square wave input	0.31	2.10	mA	
				Resonator connection	0.48	2.20	mA	
		f <sub>MX</sub> = 10 MHz Note 3, V <sub>DD</sub> = 5.0 V		Square wave input	0.21	1.10	mA	
				Resonator connection	0.28	1.20	mA	
		f <sub>MX</sub> = 10 MHz Note 3, V <sub>DD</sub> = 3.0 V	Square wave input	0.21	1.10	mA		
			Resonator connection	0.28	1.20	mA		

Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I <sub>DD3</sub> Note 6	STOP mode Note 8	T <sub>A</sub> = -40°C	0.19	0.52	μA
		T <sub>A</sub> = +25°C	0.25	0.52	μA
		T <sub>A</sub> = +50°C	0.32	2.21	μA
		T <sub>A</sub> = +70°C	0.55	3.94	μA
		T <sub>A</sub> = +85°C	1.00	7.95	μA
		T <sub>A</sub> = +105°C	5.00	40.00	μA

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). **The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.**
  - Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.**
  - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz
  - Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T<sub>A</sub> = -40 to +105° C, 2.4 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 6	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.62	3.40	mA
					V <sub>DD</sub> = 3.0 V	0.62	3.40	mA
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.50	2.70	mA
					V <sub>DD</sub> = 3.0 V	0.50	2.70	mA
			f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V	0.44	1.90	mA	
				V <sub>DD</sub> = 3.0 V	0.44	1.90	mA	
			HS (high-speed main) mode Note 6	f <sub>MX</sub> = 20 MHz Note 3, V <sub>DD</sub> = 5.0 V	Square wave input	0.31	2.10	mA
					Resonator connection	0.48	2.20	mA
		f <sub>MX</sub> = 20 MHz Note 3, V <sub>DD</sub> = 3.0 V		Square wave input	0.31	2.10	mA	
				Resonator connection	0.48	2.20	mA	
		f <sub>MX</sub> = 10 MHz Note 3, V <sub>DD</sub> = 5.0 V		Square wave input	0.21	1.10	mA	
				Resonator connection	0.28	1.20	mA	
		f <sub>MX</sub> = 10 MHz Note 3, V <sub>DD</sub> = 3.0 V	Square wave input	0.21	1.10	mA		
			Resonator connection	0.28	1.20	mA		

Symbol	Conditions	MIN.	TYP.	MAX.	Unit
I <sub>DD3</sub>	STOP mode Note 7	T <sub>A</sub> = -40°C	0.19	0.52	μA
		T <sub>A</sub> = +25°C	0.25	0.52	μA
		T <sub>A</sub> = +50°C	0.32	2.21	μA
		T <sub>A</sub> = +70°C	0.55	3.94	μA
		T <sub>A</sub> = +85°C	1.00	7.95	μA
		T <sub>A</sub> = +105°C	5.00	40.00	μA

- Notes 1.** Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. **The following points apply in the HS (high-speed main) mode.**
- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
  - The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the RTC.
- In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.
- During HALT instruction execution by flash memory.
  - When high-speed on-chip oscillator and subsystem clock are stopped.
  - When high-speed system clock and subsystem clock are stopped.
  - When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).
  - Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
HS (high-speed main) mode: 2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 32 MHz  
2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V@1 MHz to 16 MHz

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$

7. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^\circ\text{C}$