Date: Apr. 8, 2026

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0584A/E	Rev.	1.00
Title	RH850/U2Bx, U2Bx-E Clock Monitor Backup Clock Limitation		Information Category	Technical Notification		
Applicable Product	RH850/U2B-FCC, U2B6, U2B10, U2B24-E EVA, U2B24-E, U2B16-E, U2B12-E, U2B6-E	Lot No. All	Reference Document	R01UH1046EJ0110 (RH850/U2B-E Group User's Manual: Hardware) R01UH0923EJ0120 (RH850/U2B Group User's Manual: Hardware)		

[Overview]

When System Reset 2 occurs, a System Clock Gear Down is performed inside the CHIP. However, if a CLMA error occurs during the System Clock Gear Down process after System Reset 2, the gear-down procedure may not be completed, which can disturb the CHIP from continuing its operation.

[Applicable Product]

RH850 / U2B-FCC, U2B6, U2B10, U2B24-E EVA, U2B24-E, U2B16-E, U2B12-E, U2B6-E

[Phenomenon]

- **Condition**

When the following conditions are configured and System Reset 2 occurs.

CLMA backup clock function	MOSC frequency	CLMA3 setting	CLMA15 setting	Phenomenon A
Disable	X	X	X	Not Applicable
Enable	40MHz, 25MHz, 24MHz	X	X	Not Applicable
	20MHz	Disable	X	Not Applicable
		Enable	Disable	Applicable
			Enable	Not Applicable
	16MHz	Disable	Disable	Not Applicable
			Enable	Applicable
		Enable	X	Applicable

- **Phenomenon**

➢ **Phenomenon A: Clock Stop)** After System Reset 2 factor occurs, the clock gear down process is executed inside the chip. A CLMA error occurs during the clock gear down process. And the internal reset process will be initiated by the CLMA error without waiting for the completion of clock gear down process. As the result, clock gear down process (clock gear down of CLK_PLLO/CLK_SSCGO and clock selection from CLK_PLLO/CLK_SSCGO to CLK_IOSC) may not be performed correctly, and the chip may not be able to continue operating.

The above case occurs after System Reset 2 depends on the state of the internal clock divider and the timing of CLMA error detection.

- **Recovery**

  In case of chip could not continue (Phenomenon A), use an External Reset to recover.

- **Work Around**

  - Using MOSC = 20MHz case:

    Set the CLMA15 to enable (CLMA15CTL.CKMA15CLME=1) or

    Set the Backup clock to disable (CLMABCE. CLMABCE = 0).

  - Using MOSC = 16MHz case:

    Set the Backup clock to disable (CLMABCE. CLMABCE = 0).

[Change point] (Only for RH850/U2B Group User's Manual: Hardware)

The following description will be changed in User's Manual (Red character)

Section 16 Clock Monitor (CLMA)

16.5 Registers

16.5.6 CLMABCE — Clock Monitor Backup Clock Enable Register

<Before>

16.5.6 CLMABCE — Clock Monitor Backup Clock Enable Register

This register is a backup clock (CLK_IOSC) switching control register.

When CLMA0, CLMA3 or CLMA15 detects an error, clock switching operation occurs.

For switching points, see **Section 15, Clock Controller**.

Access: This register can be read or written in 8-bit units

Address: $FF98\_9008_H$

Value after reset: 00_H

Bit	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	CLMABCE
Value after reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R/W

Table 16.12 CLMABCE Register contents

Bit Position	Bit Name	Function
7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	CLMABCE	Backup clock switching control 0: Disable the backup clock function 1: Enable the backup clock function

<After>

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R/W	R	R	R	R	R	R	R	R/W

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7 to 1	Reserved	When read, the value after reset is returned. When writing, write the value after reset.
0	CLMABCE	Backup clock switching control 0: Disable the backup clock function 1: Enable the backup clock function *1

*1 : When MOSC = 20 MHz (with CLMA15 disabled) or when MOSC = 16 MHz, do not set it to 1.

[Judgement Flow]