Date: Aug. 5, 2020

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RH8-B0295A/E	Rev.	1.00
Title	RH850/E2x, U2Ax sDMAC address error detection limitations		Information Category	Technical Notification		
Applicable Product	RH850/E2x-FCC1, E2M RH850/E2x-FCC2, E2UH, E2H RH850/U2A-EVA, U2A16, U2A8	Lot No. All lot	Reference Document	R01UH0641EJ0130 (E2x-FCC1, E2M) R01UH0770EJ0100 (E2x-FCC2, E2UH, E2H) R01UH0864EJ0070 (U2A-EVA, U2A16, U2A8)		

Limitations of sDMAC address error detection are added or modified as follows:

Red character: Added

Blue character: Modified

1. User's Manual Update: E2x

7.3.8 DMAjSAR_n — DMA Source Address Register

DMAjSAR_n is a 32-bit read/write register that specifies the source address of DMA transfer. During DMA transfer, this register indicates the next source address.

When the selected source address mode is "increment" (SM bit in DMAjTMR_n register is 01_B), the source address can be specified on a byte boundary. Otherwise the source address must be specified on the transaction size boundary (STS bit in DMAjTMR_n register).

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: In case of using the gather transfer function, this register must be set to a multiple of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

7.3.17 DMAjGIAI_n — DMA Gather Inner Address Increment Register

DMAjGIAI_n is a 32-bit read/write register that specifies the source address increment for the inner loop of a gather transfer.

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GIAI[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GIAI[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: This register must be set to a multiple of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

7.3.18 DMAjGOAI_n — DMA Gather Outer Address Increment Register

DMAjGOAI_n is a 32-bit read/write register that specifies the source address increment for the outer loop of a gather transfer.

Value after reset: 0000 0000H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GOAI[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GOAI[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: This register must be set to a multiple of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

7.5 Usage Notes

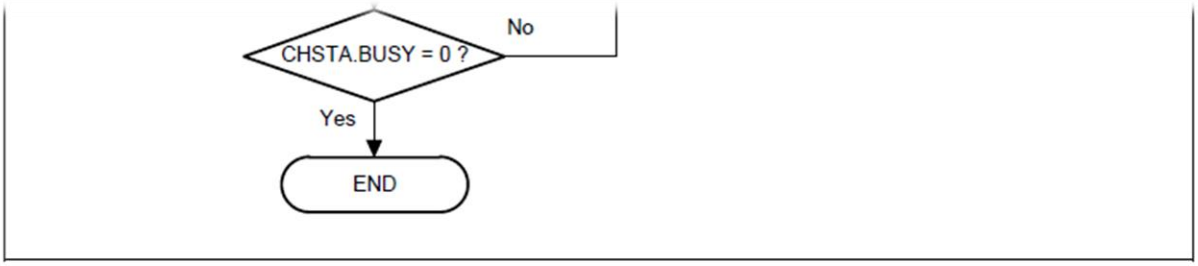

Figure 7.29 Example of DMA Transfer Stop and Restart Processing

~~**(4) Impact of Transfer Unit Size on Addresses and Offsets**~~

~~The general recommendation is to set the base addresses (SAR, DAR) and address increments (GIAI, GOAI, SIAI, SOAI) to a multiple of the related transfer unit size (STS, DTS). If this recommendation is not followed, byte transfers are used instead. This reduces the performance significantly.~~

(4) Restriction and Impact on the Transfer Unit Size on Addresses and Offsets

The general recommendation is to set the base address (SAR, DAR) and the scatter address increments (SIAI, SOAI) to a multiple of the related transfer unit size (STS, DTS). If this recommendation is not followed, the byte transfers are used instead. This reduces the performance significantly.

In case of using the gather transfer function, the DMA Source Address Register (DMAjSAR_n), the DMA Gather Inner Address Increment Register (DMAjGIAI_n) and the DMA Gather Outer Address Increment Register (DMAjGOAI_n) must be set to multiples of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

2. User's Manual Update: U2Ax

7.3.8 DMAjSAR_n — DMA Source Address Register n

DMAjSAR_n is a 32-bit read/write register that specifies the source address of DMA transfer. During DMA transfer, this register indicates the next source address.

When the selected source address mode is "increment" (SM bit in DMAjTMR_n register is 01_B), the source address can be specified on a byte boundary. Otherwise the source address must be specified on the transaction size boundary (STS bit in DMAjTMR_n register).

Access: DMAjSAR_n register can be read or written in 32-bit units

Address: <SDMACj_base> + (n × 80_H) + 2000_H

Value after reset: $0000\ 0000_H$

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: In case of using the gather transfer function, this register must be set to a multiple of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

7.3.17 DMAjGIAI_n — DMA Gather Inner Address Increment Register n

DMAjGIAI_n is a 32-bit read/write register that specifies the source address increment for the inner loop of a gather transfer.

Access: DMAjGIAI_n register can be read or written in 32-bit units
Address: <SDMACj_base> + (n × 80_H) + 2020_H
Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GIAI[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GIAI[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: This register must be set to a multiple of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

7.3.18 DMAjGOAI_n — DMA Gather Outer Address Increment Register n

DMAjGOAI_n is a 32-bit read/write register that specifies the source address increment for the outer loop of a gather transfer.

Access: DMAjGOAI_n register can be read or written in 32-bit units
Address: <SDMACj_base> + (n × 80_H) + 2024_H
Value after reset: 0000 0000_H

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GOAI[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GOAI[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: This register must be set to a multiple of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

7.5 Usage Notes

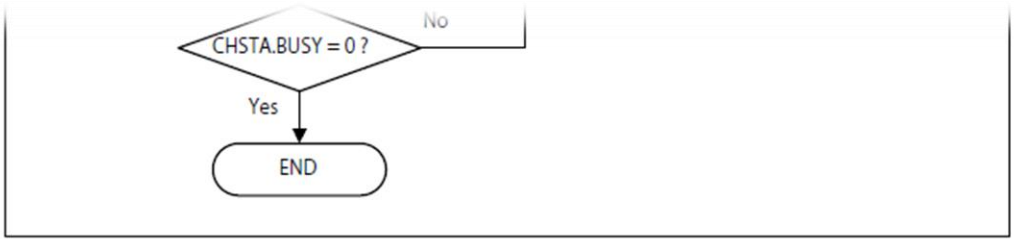

Figure 7.29 Example of DMA Transfer Stop and Restart Processing

~~(4) Impact of Transfer Unit Size on Addresses and Offsets~~

~~The general recommendation is to set the base addresses (SAR, DAR) and address increments (GIAI, GOAI, SIAI, SOAI) to a multiple of the related transfer unit size (STS, DTS). If this recommendation is not followed, byte transfers are used instead. This reduces the performance significantly.~~

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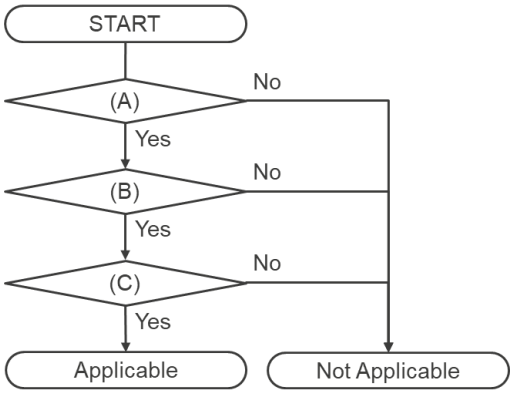
The general recommendation is to set the base address (SAR, DAR) and the scatter address increments (SIAI, SOAI) to a multiple of the related transfer unit size (STS, DTS). If this recommendation is not followed, the byte transfers are used instead. This reduces the performance significantly.

In case of using the gather transfer function, the DMA Source Address Register (DMAjSAR_n), the DMA Gather Inner Address Increment Register (DMAjGIAI_n) and the DMA Gather Outer Address Increment Register (DMAjGOAI_n) must be set to multiples of DMA source transaction size which is set to STS bit in the DMAjTMR_n register.

3. Judgement flow



(A)	Is a DMA transfer with two or more channels executed at the same time ?
(B)	Is the gather transfer function used (DMAjSGCR_n.GEN = 1) ?
(C)	Is an unaligned DMA transfer from the transfer source executed ? *1

*1 For the details of condition (C), see the following table.

DMAjTMR_n.STS	DMAjSAR_n / DMAjGIAI_n / DMAjGOAI_n
0001: 2-byte unit transfer	Either set value is except the multiple of 2 among above registers.
0010: 4-byte unit transfer	Either set value is except the multiple of 4 among above registers.
0011: 8-byte unit transfer 0100: 16-byte unit transfer 0101: 32-byte unit transfer 0110: 64-byte unit transfer	Either set value is except the multiple of 8 among above registers.

Fin.