Date: May 24, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0472A/E	Rev.	1.00
Title	RH850/E2x no CK clock issue		Information Category	Technical Notification		
Applicable Product	RH850/E2x serise E2x-FCC1, E2M, E2x-FCC2, E2H, E2UH	Lot No. All	Reference Document	RH850/E2x-FCC1 Group: R01UH0641EJ0130 R01UH0725EJ0130 (FCC1) R01UH0778EJ0130 (E2M) RH850/E2x-FCC2 Group: R01UH0770EJ0121 R01UH0793EJ0120 (FCC2) R01UH0830EJ0120 (E2UH) R01UH0861EJ0120 (E2H)		

This technical update reports the following 1 issue in RH850/E2x series products.

■ Issue

Summary

CK might not output depending on several factors.

Initialization of the “Divider 2” may fail.

Section 15 Clock Controller, 15.2.2 Block Diagram

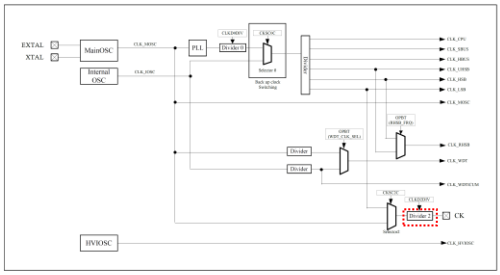

Figure 15.1 Block Diagram of Clock Controller

HWUM revision

RH850/E2x-FCC1 Group (E2M)

<Before>

RH850/E2x-FCC1 Section 15 Clock Controller

15.4.2 External Clock Output Pins (CK)

The device provides an external clock that can be used as clock supply for other external circuits. For details, see **Section 15.3.6, CLKDnDIV — Clock Divider Divisor Register (n = 2)**, **Section 15.3.7, CLKDnSTAT — Clock Divider Status Register (n = 2)**, **Section 15.3.10, CKSCnC — Clock Selector Control Register (n = 2)**, and **Section 15.3.11, CKSCnS — Clock Selector Status Register (n = 2)**.

- Clock signals can be output from the external pin CK.
- Output clock frequencies can be divided by the divider by configuring register settings.
- The source of the external clock can be configured as CLK_MOSC or CLK_LSB.
- It is recommended that the external clock be configured after clock gearup is complete.

NOTES

1. Stop the external clock before changing the clock source.
2. CLK_LSB becomes the backup clock if changing to a backup clock was triggered by an error detected in CLMA.

<After>

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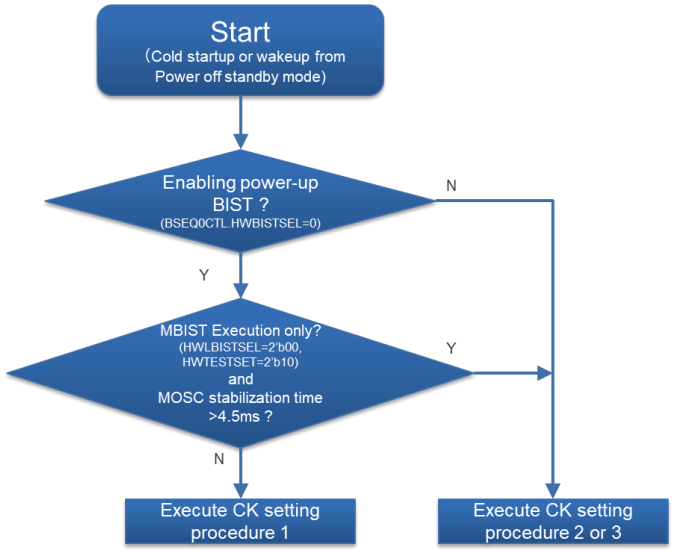
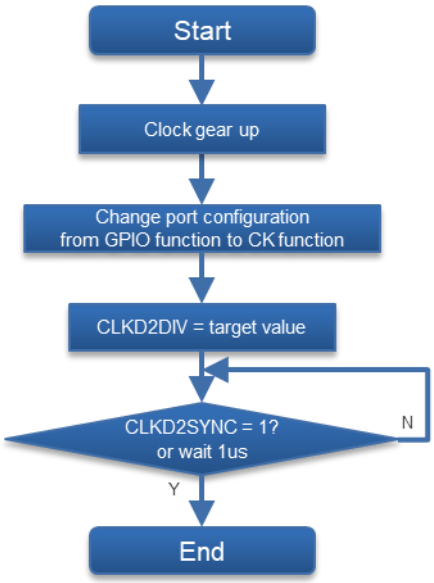
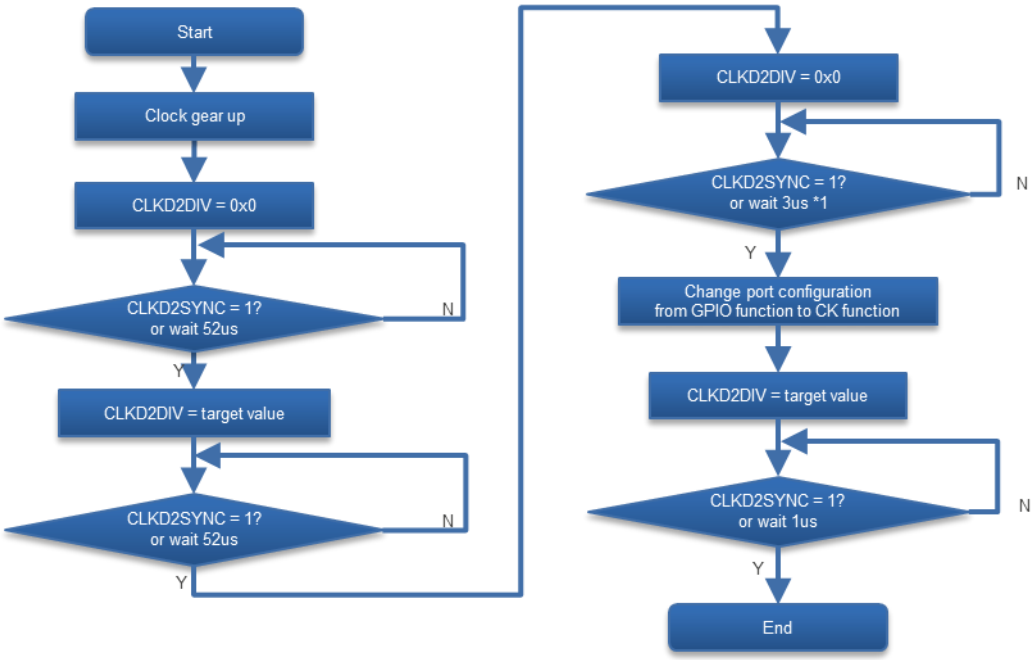
- Please execute the setting procedure according to the use case.



<CK setting procedure 1>
"CK setting procedure 1" is the normal way to set the CK function.

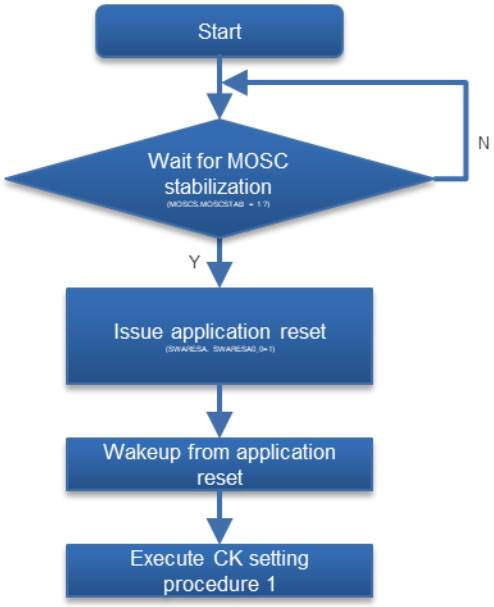


<CK setting procedure 2>
Please execute the register settings for CK in the following specific procedure if HW BIST is not run at startup.



(*1) If CLKD2DIV=5, the wait time can be 1us.
3us is the maximum time at any other settings.

<CK setting procedure 3>
The specific procedure shown in "CK setting procedure 2" is not necessary if an application reset is performed as described in Section 10.2.8 after MOSC stabilization has been confirmed.



NOTES
•Please change the clock source after MOSC stabilization.
•Stop the external clock before changing the clock source.
•CLK_LSB becomes the backup clock if changing to a backup clock was triggered by an error detected in CLMA.

Electrical Characteristics revision

RH850/E2x-FCC1

<Before>

1.3.4 Clock Timing

1.3.4.1 Main Oscillator Characteristics

Table 1.21 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
MainOsc oscillation stabilization time	t_{MSTB}	Crystal	—	—	5	ms

<After>

1.3.4 Clock Timing

1.3.4.1 Main Oscillator Characteristics

Table 1.21 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
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Note 1. If the external clock output pins (CK) function use, it has a restriction. Please refer to “15.4.2. External Clock Output Pins (CK).

RH850/E2M

<Before>

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HWUM revision

RH850/E2x-FCC2 Group (E2H/E2UH)

<Before>

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1. Stop the external clock before changing the clock source.
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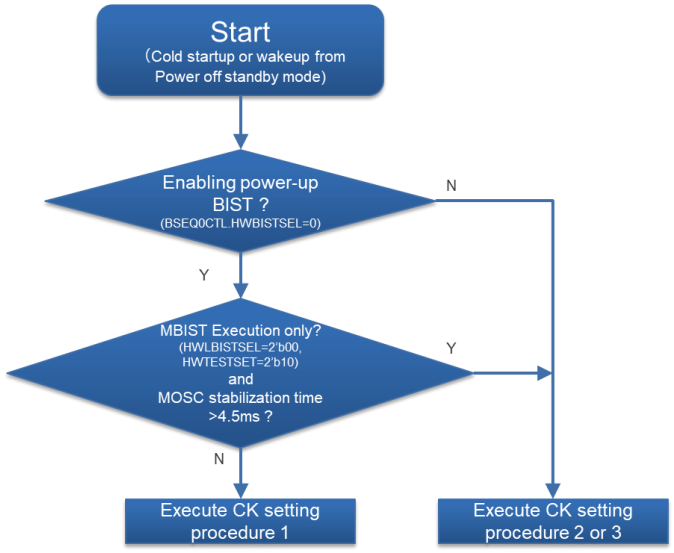

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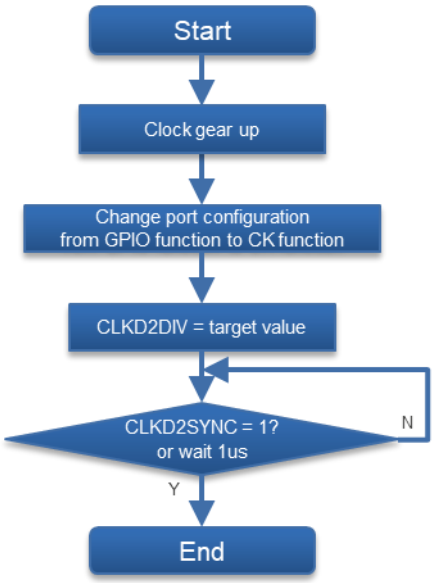

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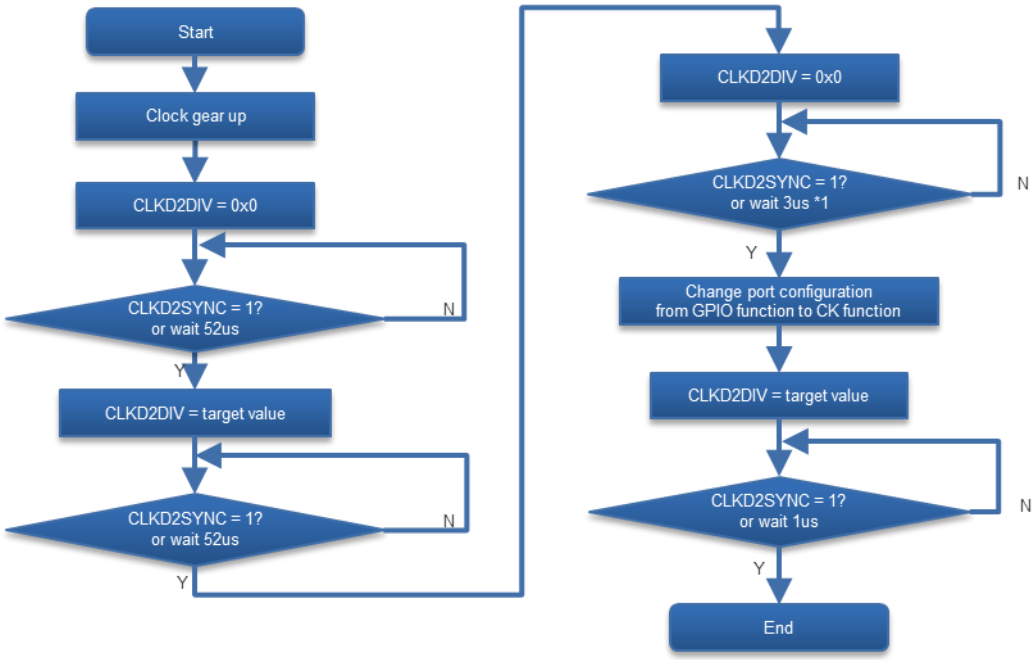

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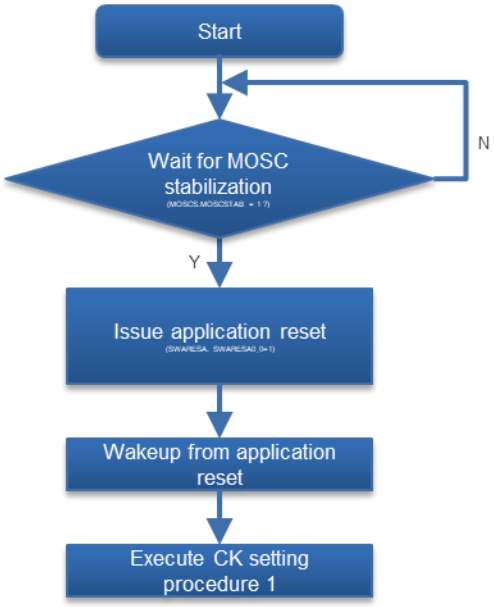

NOTES
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•Stop the external clock before changing the clock source.
•CLK_LSB becomes the backup clock if changing to a backup clock was triggered by an error detected in CLMA.

Electrical Characteristics revision

RH850/E2x-FCC2

<Before>

1.3.4 Clock Timing

1.3.4.1 Main Oscillator Characteristics

Table 1.21 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
MainOsc oscillation stabilization time	t_{MSTB}	Crystal	—	—	5	ms

<After>

1.3.4 Clock Timing

1.3.4.1 Main Oscillator Characteristics

Table 1.21 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
MainOsc oscillation stabilization time	t_{MSTB}	Crystal	—	—	5 *1	ms

Note 1. If the external clock output pins (CK) function use, it has a restriction. Please refer to “15.4.2. External Clock Output Pins (CK).

RH850/E2UH

<Before>

1.3.3 Clock Timing

1.3.3.1 Main Oscillator Characteristics

Table 1.20 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
MainOsc oscillation stabilization time	t_{MSTB}	Crystal	—	—	5	ms

<After>

1.3.3 Clock Timing

1.3.3.1 Main Oscillator Characteristics

Table 1.20 Main Oscillator Characteristics (1/3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
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RH850/E2H

<Before>

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1.3.3.1 Main Oscillator Characteristics

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Item	Symbol	Condition	Min.	Typ.	Max.	Unit
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1.3.3.1 Main Oscillator Characteristics

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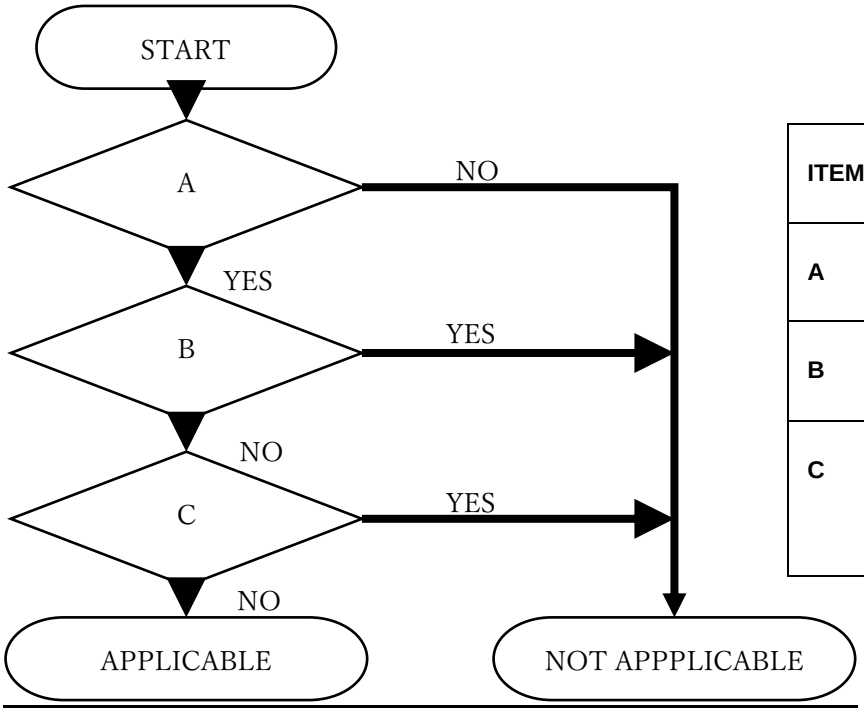
Note 1. If the external clock output pins (CK) function use, it has a restriction. Please refer to “15.4.2. External Clock Output Pins (CK).

Judgement flow



ITEM	DESCRIPTION
A	Is the CK function used?
B	Is BIST run at power-up in except MBIST Execution only?
C	Is BIST run at power-up in MBIST Execution only and MOSC stabilization time* < 4.5ms? *t_{MSTB}

40.6.2.20 BSEQ0SEL — BIST Scenario Select Register

Table 40.429 BIST scenario use case

	HWLBISTSEL [1:0]*1	HWTESTSET [1:0]*1	Function	Run time*2	Target ASIL*3
Item C	00	10	MBIST Execution	5 ms (MBIST 5ms)	—
Item B	01	11	LBIST and MBIST Execution	10 ms (LBIST 5 ms, MBIST 5 ms)	ASIL B
	10	01	LBIST Execution	15 ms (LBIST 15 ms)	ASIL D
	11	11	LBIST and MBIST Execution	20 ms (LBIST 15 ms, MBIST 5 ms)	ASIL D

Fin.