Date: Jun. 3, 2020

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0280A/E	Rev.	1.00
Title	RH850/D1Mx Additional descriptions relating to JPEG Codec unit		Information Category	Technical Notification		
Applicable Product	RH850/D1M1(H) RH850/D1M1A RH850/D1M1-V2 RH850/D1M2(H)	Lot No. All	Reference Document	RH850/D1L/D1M Group User's Manual: Hardware Rev.2.20 (R01UH0451EJ0220)		

There is some missing information for JPEG Codec unit (JCUA) on user's manual.

This RENESAS Technical update will mention of them.

1. Description

Description on user's manual will be updated as follows. Modification points are used red color.

Note 6 is added to JCUA: "Note 6: Write path must not be used."

Table 14.11 D1M1(H) connection matrix (Page 746)

	Master									
	CPU Sybsystem						Sprite Engine			
	CPU I/F		Global I/F							
	CPU	DMA	OCD	GPU2D	ETNB	JCUA	RLE Unit*2	Sprite Unit 0*3	Sprite Unit 1*4	Sprite Unit 2*5
Slaves	MSTID1	MSTID2	MSTID0	MSTID4	MSTID6	MSTID5	MSTID8	MSTID9	MSTID 10	MSTID 11
CPU Subsystem global I/F*1	-	-	-	R/W*6	R/W*6	R/W*6	R/W	R/W	R/W*6	R/W

Table 14.12 D1M1-V2 connection matrix (Page 750)

	Master									
	CPU Sybsystem						Sprite Engine			
	CPU I/F		Global I/F							
	CPU	DMA	OCD	GPU2D	ETNB	JCUA	RLE0/ SPEA3*2	RLE1/ SPEA0*3	RLE2/ SPEA1*4	RLE3/ SPEA2*5
Slaves	MSTID 1	MSTID 2	MSTID 0	MSTID 4	MSTID 6	MSTID 5	MSTID 8	MSTID 9	MSTID 10	MSTID 11
CPU Subsystem global I/F*1	-	-	-	R/W*6	R/W*6	R/W*6	R/W	R/W	R/W*6	R/W

Table 14.13 D1M1A connection matrix (Page 754)

	Master										
	CPU Sybsystem							Sprite Engine			
	CPU I/F		Global I/F								
	CPU	DMA	OCD	GPU2D	ETNB	JCUA	NFMA	RLE0/ SPEA3*2	RLE1/ SPEA0*3	RLE2/ SPEA1*4	RLE3/ SPEA2*5
Slaves	MSTID 1	MSTID 2	MSTID 0	MSTID 4	MSTID 6	MSTID 5	MSTID 7	MSTID 8	MSTID 9	MSTID 10	MSTID 11
CPU Subsystem global I/F*1	-	-	-	R/W*6	R/W*6	R/W*6		R/W	R/W	R/W*6	R/W

Table 14.14 D1M2(H) connection matrix (Page 759)

	Master										
	CPU Sybsystem							Sprite Engine			
	CPU I/F		Global I/F								
	CPU	DMA	OCD	GPU2D	MLBB	ETNB	JCUA	RLE Unit*2	Sprite Unit 0*3	Sprite Unit 1*4	Sprite Unit 2*5
Slaves	MSTID 1	MSTID 2	MSTID 0	MSTID 4	MSTID 7	MSTID 6	MSTID 5	MSTID 8	MSTID 9	MSTID 10	MSTID 11
CPU Subsystem global I/F*1	-	-	-	R/W*6	R/W*6	R/W*6	R/W*6	R/W	R/W	R/W*6	R/W

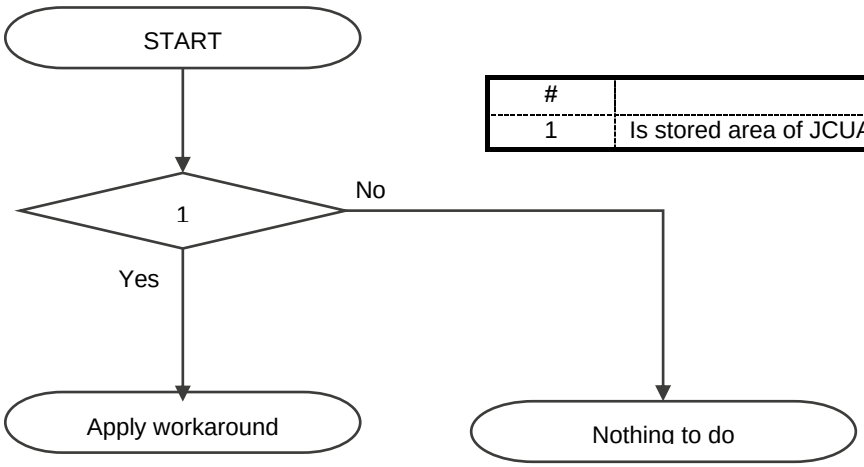
2. Workaround

When execution results of JCUA is stored to LRAM, change stored area to VRAM.

3. Final handling

The above updates will be applied to the next revision of RH850/D1M/D1L Group User's Manual: Hardware Rev.2.20.

4. Judgement flow



#	Condition
1	Is stored area of JCUA located on LRAM?