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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0246C/E	Rev.	3.00
Title	RH850/C1M-A1, RH850/C1M-A2 User's Manual Hardware Rev.1.20 Errata		Information Category	Technical Notification		
Applicable Product	RH850/C1M-A1 RH850/C1M-A2	Lot No. -	Reference Document	Refer to the below		

1. Explanation

This document is errata of RH850/C1M-A1, RH850/C1M-A2 User's Manual Hardware Rev.1.20.

No.1 to No.15 have already been notified on the previous edition of TN-RH8-B0246A/E.

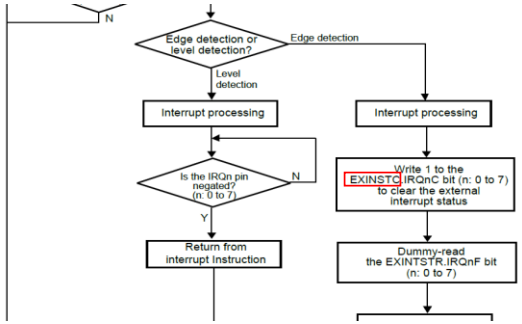
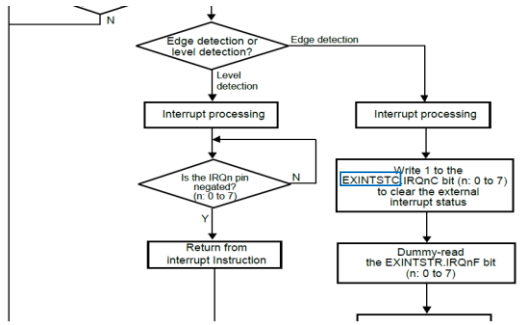
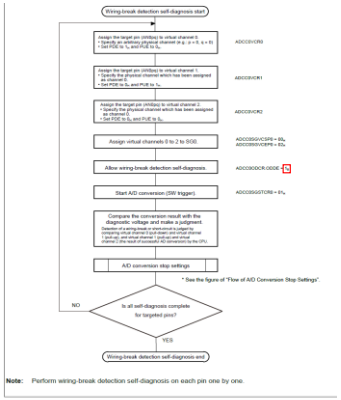
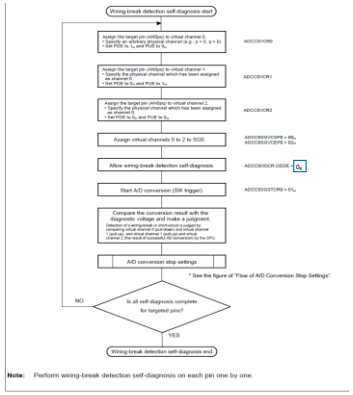
No.16 to No.53 have already been notified on the previous edition of TN-RH8-B0246B/E.

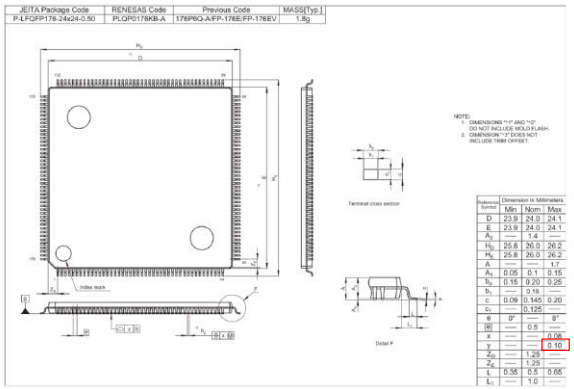
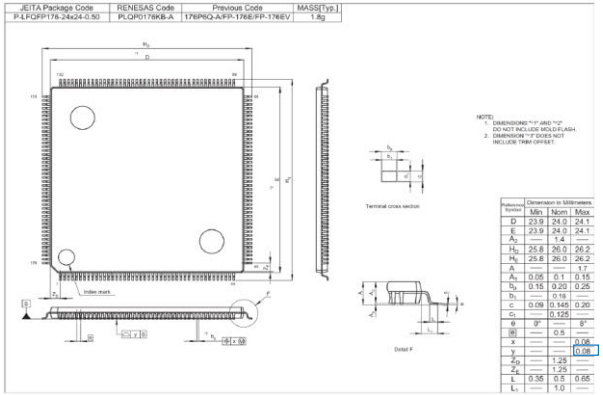
No.54 to No.71 are additional items.

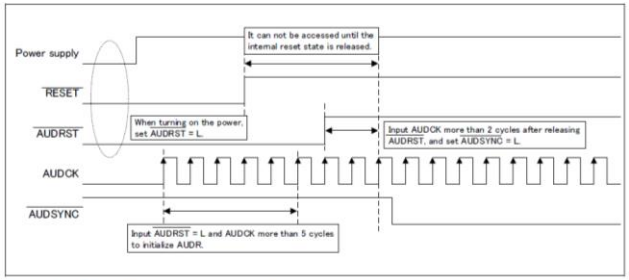
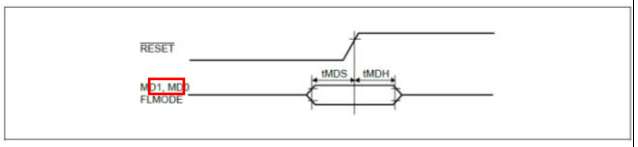
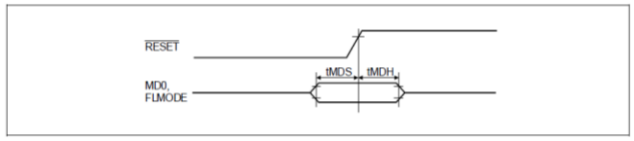
【Reference Documents】

Series	Series	Series	Rev.	Document No
RH850	C1M-A1, C1M-A2	RH850/C1M-A1, RH850/C1M-A2 User's Manual: Hardware	1.20	R01UH0607EJ0120

The changes are shown below. (Error: red, Correct: blue)

No.	PDF page (Rev.1.20)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note
1	285	Interrupt	Figure 6.1 Example of External Interrupt Processing Flow			Writing Error	–	–
2	2531	ADCC	27.4.7.3 Wiring–Break Detection Self–Diagnosis Circuit Function	27.4.7.3 Wiring–Break Detection Self–Diagnosis Circuit Function This is a function to detect a wiring–break in a pin due to solder separation. Discharge the target analog pin for the specified time in the wiring–break detection control register (ADCCnODCR register) and then perform A/D conversion. If the conversion result attenuates to approximately 0 V, you can determine that a wiring–break is present.	27.4.7.3 Wiring–Break Detection Self–Diagnosis Circuit Function This is a function to detect a wiring–break in a pin due to solder separation. If a wiring break exists the result of conversion converges approximately to AnVSS or AnVCC due to pull–down or pull–up method.	Writing Error	–	–
3	2537	ADCC	27.5.5 Procedure for Setting Wiring–Break Detection Self–Diagnosis	27.5.5 Procedure for Setting Wiring–Break Detection Self–Diagnosis Wiring–break detection is a facility for detecting wiring breaks in ANI. Both pull–down and pull–up methods are used for detection. In pull–down method, if a wiring–break occurs, the result of the AD conversion is attenuated to approximately 0V, which is detected as an abnormal value. Therefore, the user can judge that a wiring–break has been detected. In pull–up method, if a wiring–break occurs, the result of the AD conversion is booted to approximately 5V,which is detected as an abnormal value. Therefore, the user can judge that a wiring–break has been detected.	27.5.5 Procedure for Setting Wiring–Break Detection Self–Diagnosis Wiring–break detection is a facility for detecting wiring breaks in ANI. In wiring–break detection mode, a pull–down or pull–up resistor is connected for sampling of the sample–and–hold circuits when the width of pulse is fixed (18 states). In pull–down method, if a wiring–break occurs, the result of the AD conversion is attenuated to approximately AnVSS, which is detected as an abnormal value. Therefore, the user can judge that a wiring–break has been detected. In pull–up method, if a wiring–break occurs, the result of the AD conversion is booted to approximately AnVCC,which is detected as an abnormal value. Therefore, the user can judge that a wiring–break has been detected.	Writing Error	–	–
4	2538	ADCC	Figure 27.28 Flow of Wiring–Break Detection Self–Diagnostic Settings	 Figure 27.28 Flow of Wiring-Break Detection Self-Diagnostic Settings	 Figure 27.28 Flow of Wiring-Break Detection Self-Diagnostic Settings	Writing Error	–	–
5	2649	Functional Safety	Table 29.66 List of ECC Modules	Table 29.66 List of ECC Modules ECC Module Names and Register Base Addresses Master Side*1 / Checker Side*1 Supported Peripheral Function Module Name / Base Address <base_addr> RS-CANFD: Message buffer RAM (MB RAM): E7RC1M, FFC71000H, E7RC1C, FFC71200H Acceptance filter list RAM (AFL RAM): E7RC2M, FFC71400H, E7RC2C, FFC71600H CSIH: CSIH0: E7CS0M, FFC70000H, E7CS0C, FFC70200H CSIH1: E7CS1M, FFC70400H, E7CS1C, FFC70600H CSIH2: E7CS2M, FFC70800H, E7CS1C, FFC70A00H Note 1. Two modules (one for master and the other for checker) are provided for duplex configuration.	Table 29.66 List of ECC Modules ECC Module Names and Register Base Addresses Master Side*1 / Checker Side*1 Supported Peripheral Function Module Name / Base Address <base_addr> RS-CANFD: Message buffer RAM (MB RAM): E7RC1M, FFC71000H, E7RC1C, FFC71200H Acceptance filter list RAM (AFL RAM): E7RC2M, FFC71400H, E7RC2C, FFC71600H CSIH: CSIH0: E7CS0M, FFC70000H, E7CS0C, FFC70200H CSIH1: E7CS1M, FFC70400H, E7CS1C, FFC70600H CSIH2: E7CS2M, FFC70800H, E7CS2C, FFC70A00H Note 1. Two modules (one for master and the other for checker) are provided for duplex configuration.	Writing Error	–	–

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>6</td><td>2895</td><td>Appendix A Package Dimensions</td><td>QFP176 (standard)</td><td>・QFP176 (standard)
  </td><td>・QFP176 (standard)
  </td><td>Description Change</td><td>TN-RH8-B163A/E</td><td>–</td></tr>
<tr><td>7</td><td>2710</td><td>Functional Safety</td><td>Table 29.103 ERRSLVxxADDR Register Contents</td><td>Table 29.103 ERRSLVxxADDR Register Contents
Bit Position | Bit Name | Function
31 to 0 | ADDR[31:0] | Address at which an error has occurred.
ADDR[1:0] are fixed to 0.</td><td>Table 29.103 ERRSLVxxADDR Register Contents
Bit Position | Bit Name | Function
31 to 0 | ADDR[31:0] | Address at which an error has occurred.
ADDR[1:0] are undefined.</td><td>Description Change</td><td>TN-RH8-B0193A/E</td><td>–</td></tr>
<tr><td>8</td><td>2670</td><td>Functional Safety</td><td>29.3 Lockstep</td><td>none</td><td>29.3.3 Usage Notes
Reading a register with a value that is undefined after a reset without initializing the register may lead to a lock step compare error. Accordingly, such registers must be initialized with the desired settings.
Even if the branch instruction and the subsequent instruction is issued in parallel, the lock step compare error might be occurred by undefined register after the reset. It should be applied as specified below until the register which refer by subsequent instruction is initialized in case of branching in the preceding instruction.
● Insert the SYNCI instruction or the RIE instruction following the branch instruction.(It has to be added by assembler language. When C language is used, it could be optimized.)
Applicable branch instructions: Bcond except BR, JARL, JMP</td><td>Description Change</td><td>TN-RH8-B0183C/E</td><td>–</td></tr>
<tr><td>9</td><td>247</td><td>Operating Mode</td><td>Table 5.1 Selection of Operating Mode</td><td>Table 5.1 Selection of Operating Mode
Value Set in the Pin: MD1 | MD0 | FLMODE; Value Set in the Option Byte Register 0: STMSEL1 | STMSEL0; Operating Mode; Startup Area; Type of IF*1; Remark
0 | 0 | 0 | 0 | 0 | User boot mode | User area | The interface can be selected by OPBT2 in the option byte area. For details, see Section 35.9.2 OPBT2 — Option Byte 2 Register. | On-chip debug is available.
0 | 0 | 0 | 0 | 1 | User boot mode | User boot area | | |
0 | 0 | 0 | 1 | X | Serial programming mode | Boot area | Writer I/F (2-line UART) | Serial programming is available.
0 | 0 | 1 | X | X | Boundary scan mode | — | JTAG | Boundary scan is available.
0 | 1 | 0 | X | X | Serial programming mode | Boot area | Writer I/F (2-line UART) | Serial programming is available.
0 | 1 | 1 | X | X | Serial programming mode | Boot area | Writer I/F (3-line clock synchronous connection) | Serial programming is available.
Note: X = Don't care
Note 1. See Section 2.4.3, Pin State for the functions and states of pins when each interface is selected.</td><td>Table 5.1 Selection of Operating Mode
Value Set in the Pin: MD1*2 | MD0 | FLMODE; Value Set in the Option Byte Register 0: STMSEL1 | STMSEL0; Operating Mode; Startup Area; Type of IF*1; Remark
0 | 0 | 0 | 0 | 0 | User boot mode | User area | The interface can be selected by OPBT2 in the option byte area. For details, see Section 35.9.2 OPBT2 — Option Byte 2 Register. | On-chip debug is available.
0 | 0 | 0 | 0 | 1 | User boot mode | User boot area | | |
0 | 0 | 0 | 1 | X | Serial programming mode | Boot area | Writer I/F (2-line UART) | Serial programming is available.
0 | 0 | 1 | X | X | Boundary scan mode | — | JTAG | Boundary scan is available.
0 | 1 | 0 | X | X | Serial programming mode | Boot area | Writer I/F (2-line UART) | Serial programming is available.
0 | 1 | 1 | X | X | Serial programming mode | Boot area | Writer I/F (3-line clock synchronous connection) | Serial programming is available.
Note: X = Don't care
Note 1. See Section 2.4.3, Pin State for the functions and states of pins when each interface is selected.
Note 2. Always input low level to MD1.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>10</td><td>2795</td><td>On-Chip Debugging Unit (OCD)</td><td>Table 34.2 I/O Pins of AUDR</td><td>Table 34.2 I/O Pins of AUDR
Pin Name | I/O | Description
AUDRST | Input | AUDR reset input pin
Inputting L to this pin resets the AUDR, but it does not initialize the AUDISR, AUDMBR and AUDMBRC (described below).
When this pin is not connected, it is internally pulled-down.</td><td>Table 34.2 I/O Pins of AUDR
Pin Name | I/O | Description
AUDRST | Input | AUDR reset input pin
Inputting L to this pin resets the AUDR.
When turning on the power, set this pin to Low regardless of the use of AUDR.
When this pin is not connected, it is internally pulled-down.
Make sure to initialize AUDR before inputting High to this pin.
CAUTION: AUDR is initialized when this pin is Low and AUDCK is input for a fixed number of cycles, but it does not initialize the AUDISR, AUDMBR and AUDMBRC (described below).
Refer to Section 34.4.4.3, Usage Notes on the AUDR Function and Section 39, Electrical Characteristics for the number of cycles required for initialization.</td><td>Description Change</td><td>TN-RH8-B0228A/E</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>11</td><td>2807</td><td>On-Chip Debugging Unit (OCD)</td><td>34.4.4.3 Usage Notes on the AUDR Function</td><td>34.4.4.3 Usage Notes on the AUDR Function
• Do not negate the $\overline{\text{AUDSYNC}}$ pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.
• When uninitialized memory is accessed through the AUDR, a bus error may occur due to ECC error detection.</td><td>34.4.4.3 Usage Notes on the AUDR Function
• Do not negate the $\overline{\text{AUDSYNC}}$ pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.
• When uninitialized memory is accessed through the AUDR, a bus error may occur due to ECC error detection.
• Do not reset AUDR with $\overline{\text{AUDRST}}$ = L, while transferring data with AUDR ($\overline{\text{AUDSYNC}}$ = L). The data transfer of AUDR is not completed in the System Interconnect, and it may interfere with the data transfer of other bus masters.
• AUDR can not transfer data when being in external or internal reset state.
• Do not assert $\overline{\text{AUDSYNC}}$ pin for a minimum of 2 AUDCK cycles after AUDR reset release with $\overline{\text{AUDRST}}$ = H.
• The timing from power on to data transfer is shown in Figure 34.xx.
 
Figure 34.xx Timings from power on to data transfer</td><td>Description Change</td><td>TN-RH8-B0228A/E</td><td>–</td></tr>
<tr><td>12</td><td>2808</td><td>On-Chip Debugging Unit (OCD)</td><td>34.5 Cautions on Using On-Chip Debugger</td><td>none</td><td>(5) Handling of /DCUTRSTpin at power on
Set the /DCUTRSTpin to the low level at power on, regardless of whether on-chip debugging is used.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>13</td><td>2867</td><td>Electrical Characteristics</td><td>Figure 39.5 Control Signal Timing</td><td> 
Figure 39.5 Control Signal Timing</td><td> 
Figure 39.5 Control Signal Timing</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

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<tr><td>14</td><td>2884</td><td>Electrical Characteristics</td><td>Table 39.30 AUD RAM Monitor Timing</td><td>Table 39.30 AUD RAM Monitor Timing
Conditions: Tj = – 40ºC to 150ºC, CL = 30 pF
<table><tr><th>Item</th><th>Symbol</th><th>Min.</th><th>Max.</th><th>Unit</th></tr><tr><td>AUDCK cycle time (monitor mode)</td><td>tAUCKMcyc</td><td>50</td><td>—</td><td>ns</td></tr><tr><td>AUDCK high-level width (monitor mode)</td><td>tAUCKMH</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDCK low-level width (monitor mode)</td><td>tAUCKML</td><td>0.4 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>AUDRST setup time (monitor mode, vs. AUDCK↑)</td><td>tAURSTMS</td><td>30</td><td>—</td><td>ns</td></tr><tr><td>AUDRST input pulse width (monitor mode)</td><td>tAURSTMW</td><td>5 × tAUCKMcyc</td><td>—</td><td>ns</td></tr><tr><td>Monitor data output delay time (to AUDCK ↑)</td><td>tAUDTMD</td><td>—</td><td>35</td><td>ns</td></tr><tr><td>Monitor data input setup time (to AUDCK ↑)</td><td>tAUDTMS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>Monitor data input hold time (from AUDCK ↑)</td><td>tAUDTMH</td><td>5</td><td>—</td><td>ns</td></tr><tr><td>AUDSYNC input setup time (vs. AUDCK ↑)</td><td>tAUDSYS</td><td>15</td><td>—</td><td>ns</td></tr><tr><td>AUDSYNC input hold time (vs. AUDCK ↑)</td><td>tAUDSYH</td><td>5</td><td>—</td><td>ns</td></tr></table></td><td>Table 39.30 AUD RAM Monitor Timing
Conditions: Tj = – 40ºC to 150ºC, CL = 30 pF
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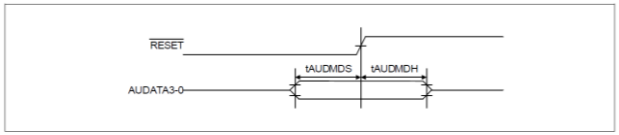
<tr><td>15</td><td>2884</td><td>Electrical Characteristics</td><td>39.3.12 AUD RAM Monitor</td><td>none</td><td> 
Figure 39.xx Timing to reflect settings on AUDISR</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>16</td><td>63</td><td>Overview</td><td>Table 1.1 Overview of Products (2/2)</td><td><table><tr><td>Motor control</td><td>R/D converter (RDC3A)</td><td>2 units</td><td>1 unit</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): Number of units</td><td>1 unit (2 channels)</td><td>1 unit (2 channels)</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): SubCPU frequency</td><td>320 MHz</td><td>240 MHz</td></tr></table></td><td><table><tr><td>Motor control</td><td>R/D converter (RDC3A)</td><td>2 units</td><td>1 unit</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): Number of units</td><td>1 unit (2 channels)</td><td>1 unit (1 channel)</td></tr><tr><td></td><td>Enhanced motor control unit (EMU3): SubCPU frequency</td><td>320 MHz</td><td>240 MHz</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>17</td><td>157</td><td>Pins</td><td>Table 2.64 Example Handling of Unused Pins (2/2)</td><td><table><tr><th>Category</th><th>Pins</th><th>IO</th><th>Example handling of unused pins</th><th>Internal pull-up/pull-down resistor</th></tr><tr><td>Debug system (NEXUS/LPD)</td><td>DCUTDI</td><td>I</td><td>• Leave the pin open.
• Separately connect the pin with VCC via a resistor.
(Serial programming mode is disabled.)</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>DCUTDO</td><td>O</td><td>• Leave the pin open.
(Serial programming mode is disabled.)</td><td>None</td></tr><tr><td></td><td>DCUTCK</td><td>I</td><td>• Leave the pin open.
• Separately connect the pin with VCC via a resistor.
(Serial programming mode is disabled.)</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>DCUTMS</td><td>I</td><td>• Leave the pin open.
• Separately connect the pin with VCC via a resistor.</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>DCUTRST</td><td>I</td><td>Separately connect the pin with VSS via a resistor.</td><td>An internal pull-down resistor is included.</td></tr><tr><td></td><td>DCURDY</td><td>O</td><td>Leave the pin open.</td><td>None</td></tr></table></td><td><table><tr><th>Category</th><th>Pins</th><th>IO</th><th>Example handling of unused pins</th><th>Internal pull-up/pull-down resistor</th></tr><tr><td>Debug system (NEXUS/LPD)</td><td>DCUTDI</td><td>I</td><td>• Leave the pin open.
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• Separately connect the pin with VCC via a resistor.</td><td>An internal pull-up resistor is included.</td></tr><tr><td></td><td>DCUTRST</td><td>I</td><td>Separately connect the pin with VSS via a resistor.</td><td>An internal pull-down resistor is included.</td></tr><tr><td></td><td>DCURDY</td><td>O</td><td>Leave the pin open.</td><td>None</td></tr></table></td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>18</td><td>160</td><td>CPU System</td><td>Table 3.1 Peripheral Group Configuration (1/4)</td><td>Table 3.1 Peripheral Group Configuration (1/4)
<table><tr><th>Peripheral Group</th><th>Module Name*1</th></tr><tr><td>CPU</td><td>INTC1</td></tr><tr><td></td><td>IPIRSS</td></tr><tr><td></td><td>IPG</td></tr><tr><td></td><td>MEV</td></tr><tr><td></td><td>PEG</td></tr><tr><td></td><td>SEG</td></tr><tr><td></td><td>TESTCOMP</td></tr><tr><td>CPU (DEBUG)</td><td>AUDR</td></tr><tr><td>0</td><td>APDP[INTC2]</td></tr><tr><td></td><td>APDP[PDMA]</td></tr><tr><td></td><td>DMASS</td></tr><tr><td></td><td>ECCCPU1</td></tr><tr><td></td><td>ECCCPU2</td></tr><tr><td></td><td>ECCEEP</td></tr><tr><td></td><td>ECCEEPC</td></tr><tr><td></td><td>ECCFLI</td></tr><tr><td></td><td>ECCGRAM</td></tr><tr><td></td><td>ECCIC1</td></tr><tr><td></td><td>ECCIC2</td></tr><tr><td></td><td>FACI[FCUFAREA*2]</td></tr><tr><td></td><td>FLASH[FRDCYCLD]</td></tr><tr><td></td><td>INTC2</td></tr><tr><td></td><td>MGDGR</td></tr><tr><td></td><td>MISG (CPU1, CPU2)</td></tr><tr><td></td><td>PBG[PBG0, PBG1]</td></tr><tr><td></td><td>ICUSE</td></tr><tr><td></td><td>DataFlash</td></tr></table></td><td>Table 3.1 Peripheral Group Configuration (1/4)
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</table>

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>19</td><td>213</td><td>CPU</td><td>Table 3.63 PEG Register Base Address: FFFE E600H</td><td>
<table>
<tr><th>Address Offset</th><th>Size (byte)</th><th>Register Name</th><th>Symbol</th><th>Permission</th><th>R/W</th><th colspan="4">Operable Bit</th><th>Value after Reset</th></tr>
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<tr><td>+00C$_H$</td><td>2</td><td>PE guard PEID&SPID master decision control register</td><td>PEGSP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>—</td><td>0000$_H$</td></tr>
<tr><td>+080$_H$</td><td>4</td><td>PE guard area mask setting register 0</td><td>PEGG0MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
<tr><td>+084$_H$</td><td>4</td><td>PE guard area base setting register 0</td><td>PEGG0BA</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>*1</td></tr>
<tr><td>+088$_H$</td><td>4</td><td>PE guard area SPID setting register 0</td><td>PEGG0SP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+08C$_H$</td><td>4</td><td>PE guard area PEID setting register 0</td><td>PEGG0PE</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+090$_H$</td><td>4</td><td>PE guard area mask setting register 1</td><td>PEGG1MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
<tr><td>+094$_H$</td><td>4</td><td>PE guard area base setting register 1</td><td>PEGG1BA</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>*1</td></tr>
<tr><td>+098$_H$</td><td>4</td><td>PE guard area SPID setting register 1</td><td>PEGG1SP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+09C$_H$</td><td>4</td><td>PE guard area PEID setting register 1</td><td>PEGG1PE</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0A0$_H$</td><td>4</td><td>PE guard area mask setting register 2</td><td>PEGG2MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
<tr><td>+0A4$_H$</td><td>4</td><td>PE guard area base setting register 2</td><td>PEGG2BA</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>*1</td></tr>
<tr><td>+0A8$_H$</td><td>4</td><td>PE guard area SPID setting register 2</td><td>PEGG2SP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0AC$_H$</td><td>4</td><td>PE guard area PEID setting register 2</td><td>PEGG2PE</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0B0$_H$</td><td>4</td><td>PE guard area mask setting register 3</td><td>PEGG3MK</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
<tr><td>+0B4$_H$</td><td>4</td><td>PE guard area base setting register 3</td><td>PEGG3BA</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>*1</td></tr>
<tr><td>+0B8$_H$</td><td>4</td><td>PE guard area SPID setting register 3</td><td>PEGG3SP</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0BC$_H$</td><td>4</td><td>PE guard area PEID setting register 3</td><td>PEGG3PE</td><td>—</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
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Note 1. This value is FEA0_0000$_H$ for CPU1 (PE1), FE80_0000$_H$ for CPU2 (PE2), and FE60_0000$_H$ for the SubCPU (PE3).
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<tr><td>+0A0$_H$</td><td>4</td><td>PE guard area mask setting register 2</td><td>PEGG2MK</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
<tr><td>+0A4$_H$</td><td>4</td><td>PE guard area base setting register 2</td><td>PEGG2BA</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>*1</td></tr>
<tr><td>+0A8$_H$</td><td>4</td><td>PE guard area SPID setting register 2</td><td>PEGG2SP</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0AC$_H$</td><td>4</td><td>PE guard area PEID setting register 2</td><td>PEGG2PE</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0B0$_H$</td><td>4</td><td>PE guard area mask setting register 3</td><td>PEGG3MK</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>FFE0 0000$_H$</td></tr>
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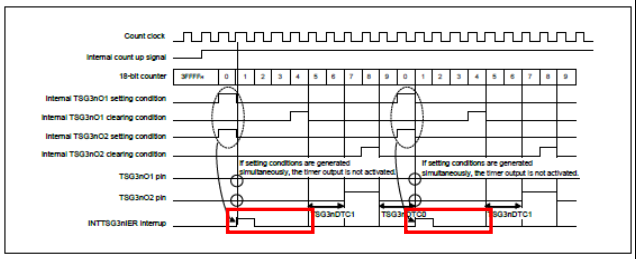
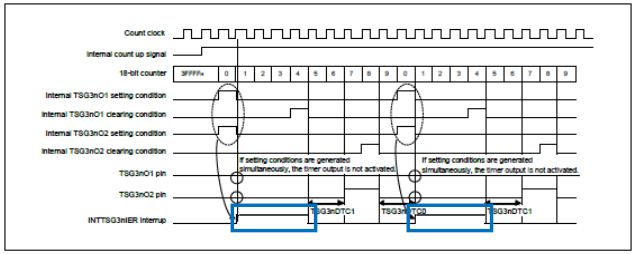
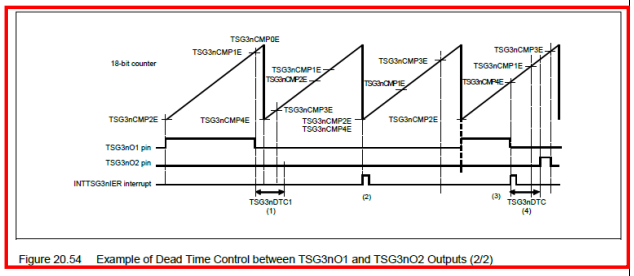
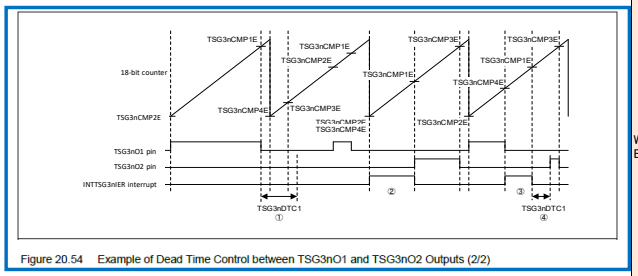
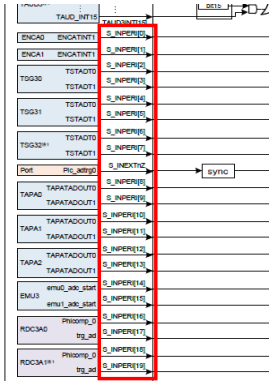
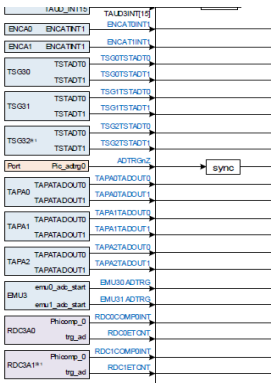
<tr><td>+0B8$_H$</td><td>4</td><td>PE guard area SPID setting register 3</td><td>PEGG3SP</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
<tr><td>+0BC$_H$</td><td>4</td><td>PE guard area PEID setting register 3</td><td>PEGG3PE</td><td>SV</td><td>R/W</td><td>—</td><td>√</td><td>√</td><td>√</td><td>0000 0000$_H$</td></tr>
</table>
Note 1. This value is FEA0_0000$_H$ for CPU1 (PE1), FE80_0000$_H$ for CPU2 (PE2), and FE60_0000$_H$ for the SubCPU (PE3).
Note 2. The registers with "SV" are only accessible in SV mode (UM = 0).
</td><td>Description Change</td><td>TN-RH8-B0281A/E</td><td>–</td></tr>
<tr><td>20</td><td>707</td><td>RLIN3</td><td>13.9 LIN Self-Test Mode</td><td>Regardless of the setting of the baud rate related registers, the baud rate operates at the LIN communication clock source/16 [bps].
(The NSPB bits in the RLN3nLWBR register should be set to 0000$_B$ or 1111$_B$.)</td><td>Regardless of the setting of the baud rate related registers, the baud rate operates at the LIN communication clock source/16 [bps].
(The NSPB bits in the RLN3nLWBR register should be set to 0000$_B$ or 1111$_B$.)
(The LPRS bits in the RLN3nLWBR register should be set to 000$_B$.)</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>21</td><td>709</td><td>RLIN3</td><td>13.9.2 Transmission in LIN Master Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxxx$_B$ *1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 000x$_B$</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>22</td><td>710</td><td>RLIN3</td><td>13.9.3 Reception in LIN Master Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxxx$_B$ *1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 000x$_B$</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>23</td><td>711</td><td>RLIN3</td><td>13.9.4 Transmission in LIN Slave Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxx0$_B$ *1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 0000$_B$</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>24</td><td>712</td><td>RLIN3</td><td>13.9.5 Reception in LIN Slave Self-Test Mode</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 xxx0$_B$ *1</td><td>● Set the baud rate, noise filter, and interrupt output related registers.
RLN3nLWBR register = 0000 0000$_B$</td><td>Description Change</td><td>TN-RH8-B0258A/E</td><td>–</td></tr>
<tr><td>25</td><td>712</td><td>RLIN3</td><td>13.9.5 Reception in LIN Slave Self-Test Mode</td><td>To execute a self-test on LIN slave reception, perform the procedure below:。</td><td>To execute a self-test on LIN slave reception, perform the procedure below:</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>26</td><td>849</td><td>RS-CANFD</td><td>14.3.13.3 RSCANnTHLPCTRm</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCANnTHLSTSm register is decremented.</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCANnTHLSTSm register is decremented by 1.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>27</td><td>1005</td><td>RS-CANFD</td><td>14.4.14.3 RSCFDnCFDTHLPCTRm</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCFDnCFDTHLSTSm register is decremented.</td><td>At this time, the THLMC[4:0] (transmit history buffer unread data counter) value in the RSCFDnCFDTHLSTSm register is decremented by 1.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>28</td><td>1032</td><td>RS-CANFD</td><td>14.8.1 Transmit Priority Determination</td><td>When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again regardless of the TPRI bit.</td><td>When messages are retransmitted due to an arbitration-lost or an error, transmit priority determination is made again according to the TPRI bit.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>29</td><td>1051</td><td>RS-CANFD</td><td>14.11.1.4 Receive Rule Setting</td><td>Up to 16 receive rules can be registered per page. Specify pages 0 to 23 (for 6-channel unit) by the AFLPN[4:0] bits in the RSCFDn(CFD)GAFLECTR register.</td><td>Up to 16 receive rules can be registered per page. Specify pages 0 to 15 (for 4-channel unit) by the AFLPN[4:0] bits in the RSCFDn(CFD)GAFLECTR register.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>30</td><td>1059</td><td>RS-CANFD</td><td>14.11.2.2 FIFO Buffer Reading Procedure</td><td>When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is
set to receive mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCFDn(CFD)RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCFDn(CFD)CFSTSk register (k = 0 to 11)) is incremented.</td><td>When received messages have been stored in one or more receive FIFO buffers or a transmit/receive FIFO buffer that is
set to receive mode or gateway mode, the corresponding message count display counter (RFMC[7:0] bits in the RSCFDn(CFD)RFSTSx register (x = 0 to 7) or CFMC[7:0] bits in the RSCFDn(CFD)CFSTSk register (k = 0 to 11)) is incremented by 1.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>31</td><td>1063</td><td>RS-CANFD</td><td>14.11.2.3 FIFO Buffer Reading Procedure by DMA Transfer</td><td>Note 1. ・For receive FIFO buffers
RCFDCnCFDRFIDx, RCFDCnCFDRFPTRx, RCFDCnCFDRFFDSTSx, RCFDCnCFDRFDFd_x
・For transmit/receive FIFO buffers
RCFDCnCFDCFIDk, RCFDCnCFDCFPTRk, RCFDCnCFDCFFDCSTSk, RCFDCnCFDCFDFd_k</td><td>Note 1. ・For receive FIFO buffers
RSCFDnCFDRFIDx、RSCFDnCFDRFPTRx、RSCFDnCFDRFFDSTSx、RSCFDnCFDRFDFd_x
・For transmit/receive FIFO buffers
RSCFDnCFDCFIDk、RSCFDnCFDCFPTRk、RSCFDnCFDCFFDCSTSk、RSCFDnCFDCFDFd_k</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>32</td><td>1160</td><td>OS Timer</td><td>17.2.2 Block Diagram</td><td>The following block diagram shows the main components of the OSTM.</td><td>The following block diagram shows the main components of the OSTM. This product does not implement OSTMnTTOUT output.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>33</td><td>1576</td><td>TSG3</td><td>20.2.1 Functional Overview</td><td>● Reload mode
– Writing to TSG3nCMP1E enables reload (the reload request flag (TSG3nRSF) is set), and allows simultaneous transfer of the values of multiple registers.
– Data can be transferred at peak/trough/peak or trough reload timing
– Reload request flag (TSG3nRSF)
– Register address assignment allowing DMA transfer</td><td>● Reload mode
– Writing to TSG3nCMP1E enables reload (the reload request flag (TSG3nRSF) is set), and allows simultaneous transfer of the values of multiple registers.
– Data can be transferred at peak/trough/peak or trough reload timing
– Reload request flag (TSG3nRSF)
– Register address assignment allowing DMA transfer
– Reload skipping</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

No.	PDF page (Rev.1.20)	Section	Chapter title (Chart title)	Error	Correct	Change reason	Notice situation	Note
34	1577	TSG3	20.2.1 Functional Overview	Reload skipping ● HT-PWM mode – 0 to 100% PWM duty cycle output is possible (with possible dead time reduction). – The LSB in the compare register can be used to append an additional pulse to the PWM output during count up, thus improving the output resolution without extra load on software.	● HT-PWM mode – 0 to 100% PWM duty cycle output is possible (with possible dead time reduction). – The LSB in the compare register can be used to append an additional pulse to the PWM output during count up, thus improving the output resolution without extra load on software.	Writing Error	–	–
35	1688	TSG3	Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)	 Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)	 Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)	Writing Error	–	–
36	1700	TSG3	Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	● TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nCMP2E (TSG3nO2 stays inactive) ● TSG3nCMP2E + TSG3nDTC0 ≥ TSG3nCMP0E + TSG3nCMP1E (TSG3nO1 stays inactive)	● TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nCMP3E (TSG3nO2 stays inactive) ● TSG3nCMP3E + TSG3nDTC0 ≥ TSG3nCMP0E + TSG3nCMP1E (TSG3nO1 stays inactive)	Writing Error	–	–
37	1700	TSG3	Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	At (4), the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected and the dead time counter starts counting. After the end of the dead time counter operation, the TSG3nO2 output becomes active.	At (4), the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected. The dead time counter starts counting after compare match with the TSG3nCMP1 register. After the end of the dead time counter operation, the TSG3nO2 output becomes active.	Writing Error	–	–
38	1700	TSG3	Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	 Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	 Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)	Writing Error	–	–
39	1812	TAPA	Table 21.17 Operation of the Hi-Z Start Trigger (TAPAnOPHS)	TAPAnOPHS | Operation 0/1 | Writing 1 to the TAPAnOPHS0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the low level.	TAPAnDCM | Operation 0/1 | Writing 1 to the TAPAnOPHS0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the low level.	Writing Error	–	–
40	1812	TAPA	Table 21.18 Operation of the Hi-Z Stop Trigger (TAPAnOPHT) during Hi-Z Control in Response to Asynchronous Input	TAPAnOPHT | Operation 0 | Writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level. 1 | If TAPAnTHASIN is at the inactive level, writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level. If TAPAnTHASIN is at the active level, writing of 1 to the TAPAnOPHT0 bit is ignored.	TAPAnDCM | Operation 0 | Writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level. 1 | If TAPAnTHASIN is at the inactive level, writing 1 to the TAPAnOPHT0 bit places the TAPAnTHZOUT0 , TAPAnTHZOUT1 , and TAPAnTHZOUT2 signals at the high level. If TAPAnTHASIN is at the active level, writing of 1 to the TAPAnOPHT0 bit is ignored.	Writing Error	–	–

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>41</td><td>2079</td><td>PIC</td><td>Figure 24.79 Block Diagram of PIC2D</td><td>  </td><td>  </td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>42</td><td>2379</td><td>RDC3A</td><td>Table 26.31 RDC3AnDIAG1 Register Contents (2/2)</td><td>8 ERRST Error Signal Reset Bit
Writing 1 to this bit resets the register bits listed below to 0. Note that each of these bits remains at 1 if an error is continuous. This bit becomes 0 after two clock cycles have elapsed following it being set to 1.
Register bits: ERHD, ERDEXC, ERDSBC, ERDSBS, ERDP2, ERDCNV, ERDR1 to 4V</td><td>8 ERRST Error Signal Reset Bit
Writing 1 to this bit resets the register bits listed below to 0. Note that each of these bits remains at 1 if an error is continuous. This bit becomes 0 after two clock cycles have elapsed following it being set to 1.
Register bits: ERHD, ERDEXC, ERDSBC, ERDSBS, ERDP2, ERDCNV, ERDR1 to 2V,ERDS1 to 4V,ERDR1 to 2G,ERDS1 to 4G</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>43</td><td>2399</td><td>RDC3A</td><td>Table 26.46 Data Selection</td><td>DATASEL[5:0] | Output Signal | Output Destination DATA[X:X]
11.1011 | 12-bit AD output code [11:0] | [11:0]
10.1111 | Control variation value [7:0] in angular conversion mode 1 | [7:0]
00.0101 | Control variation value [7:0] in angular conversion mode 0 | [7:0]</td><td>DATSEL[5:0] | Output Signal | Output Destination DATA[X:X]
11.1011 | 12-bit AD output code [11:0] | [11:0]
10.1111 | Control variation value [7:0] in angular conversion mode 1 | [7:0]
00.0101 | Control variation value [7:0] in angular conversion mode 0 | [7:0]</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>44</td><td>2405</td><td>RDC3A</td><td>Table 26.51 RDC3AnDCUR0 Register Contents</td><td>5 SYNCSL Synchronous Detection Setting in Angular Conversion Mode 1 (ADRD = 1)
b5
0: Synchronous detection setting 0
1: Synchronous detection setting 1</td><td>5 SYNCSL Synchronous Detection Setting in Angular Conversion Mode 1 (ADRD = 1)
b5
0: Synchronous detection setting 0
1: Synchronous detection setting 1
In Angular Conversion Mode 0 (ADRD = 0), set this bit to 0.</td><td>Description Change</td><td>TN-RH8-B0314A/E</td><td>–</td></tr>
<tr><td>45</td><td>2406</td><td>RDC3A</td><td>Table 26.52 RDC3AnDCUR1 Register Contents</td><td>13 DCCRSTP DC Error Correction Setting in Angular Conversion Mode 1 (ADRD = 1)
b13
0: DC correction enabled
1: DC correction disabled
Be sure to set this bit to 1 when the DC resolver is used.</td><td>13 DCCRSTP DC Error Correction Setting in Angular Conversion Mode 1 (ADRD = 1)
b13
0: DC correction enabled
1: DC correction disabled
Be sure to set this bit to 1 when the DC resolver is used.
This setting has no effect when Angular Conversion Mode 0 (ADRD = 0).</td><td>Description Change</td><td>TN-RH8-B0314A/E</td><td>–</td></tr>
<tr><td>46</td><td>2439</td><td>RDC3A</td><td>26.4.5.1 Built-in Self-Test Function</td><td>The BISTs are categorized into two groups depending on their execution timing as follows;
● Execution is possible during angle conversion and when starting up the power (short-period BIST): ADBIST, resolver signal error detection BIST, resolver signal disconnect detection BIST, power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side), sum-of-squares amplitude error detection BIST (low side)
● Execution is possible when starting up the power: angle conversion BIST, conversion error BIST</td><td>The BISTs are categorized into two groups depending on their execution timing as follows;
● Execution is possible during angle conversion and when starting up the power (short-period BIST): ADBIST, resolver signal error detection BIST, resolver signal disconnect detection BIST, power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side), sum-of-squares amplitude error detection BIST (low side)
● Execution is possible when starting up the power: angle conversion BIST, conversion error BIST
Short-period BIST can also be executed at starting up the power. However, if angle conversion BIST or conversion error BIST or both are executed at power-on, they must be executed before short-period BIST.</td><td>Description Change</td><td>TN-RH8-B0314A/E</td><td>–</td></tr>
<tr><td>47</td><td>2447</td><td>RDC3A</td><td>26.4.6.1 Period Measurement Timer</td><td>The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in the RDC3AnETCAP register. By reading the RDC3AnETCAP register, the cycle of excitation signal can be obtained.
The cycle of excitation signal can be calculated from the following formula: (RDC3AnETCAP register value + 1) × CCLK cycle (25 ns).
When the IREN bit in the RDC3AnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request
is generated if the value set in the RDC3AnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the
RDC3AnETCAP register.</td><td>The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in ET Capture bits of the RDC3AnETCAP register. By reading the RDC3AnETCAP register, the cycle of excitation signal can be obtained.
The cycle of excitation signal can be calculated from the following formula: (RDC3AnETCAP register value + 1) × CCLK cycle (25 ns).
When the IREN bit in the RDC3AnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request
is generated if the value set in ET Compare bits of the RDC3AnETCAP register matches the period measurement counter value.
The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the
RDC3AnETCAP register.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>48</td><td>2454</td><td>RDC3A</td><td>Figure 26.29 Flow of Initial Settings of the Registers</td><td>Settings for the automatic amplitude adjustment function → IRSS0, EAAOD1, IRSS1, EXOS, and SQJGT bits in the RDC3AnATMNT0 register
Set the digital operation registers → SYNCSL bit in the RDC3AnDCUR0 register ← 1
DCCRSTP bit in the RDC3AnDCUR1 register ← 1
Select the method for angle calculation → ADRD bit in the RDC3AnADRD register</td><td>Settings for the automatic amplitude adjustment function → IRSS0, EAAOD1, IRSS1, EXOS, and SQJGT bits in the RDC3AnATMNT0 register
When using Angular Conversion Mode 1(ADRD=1)
Set the digital operation registers → SYNCSL bit in the RDC3AnDCUR0 register ← 1
DCCRSTP bit in the RDC3AnDCUR1 register ← 1
Select the method for angle calculation → ADRD bit in the RDC3AnADRD register</td><td>Description Change</td><td>TN-RH8-B0314A/E</td><td>–</td></tr>
<tr><td>49</td><td>2455</td><td>RDC3A</td><td>26.6 Resolver Interface Circuit</td><td>1. RH = {(RVCC – VCOM) / (22.0 × 10^{–6})} – RIN, where VCOM = RVCC/2[V]</td><td>1. RH = {(+VEXT – VCOM) / (22.0 × 10^{–6})} – RIN, where VCOM = RVCC/2[V]</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>50</td><td>2541</td><td>ADCC</td><td>Table 27.52 Notes on Setting Registers</td><td>ADCCnTHCR, ADCCnTHACR, ADCCnTHBCR, ADCCnTHER, ADCCnTHGSR, ADCCnSGCRx, ADCCnSGVCSPx, ADCCnSGVCEPx: When setting the registers listed at left, write to the registers after they have been read. If this procedure is not followed, the written register value may not be correctly reflected in operations.</td><td>ADCCnTHCR, ADCCnTHACR, ADCCnTHBCR, ADCCnTHER, ADCCnTHGSR, ADCCnSGCRx, ADCCnSGVCSPx, ADCCnSGVCEPx: When setting the registers listed at left, write to the registers after they have been read. If writing to the register shown at the left occurs continuously without following this procedure, the written register value may not be correctly reflected in operations.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>51</td><td>2743</td><td>ECM</td><td>Table 30.8 List of Error Sources and Safety Processing (1/2)</td><td>6 | RAM | Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1) address parity error*3
7 | Local RAM (CPU1, CPU2) 1-bit ECC error and local RAM (CPU1) parity bit error*3</td><td>6 | RAM | Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1, CPU2) address parity error*3
7 | Local RAM (CPU1, CPU2) 1-bit ECC error and local RAM (CPU1, CPU2) parity bit error*3</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>52</td><td>2835</td><td>Flash Memory</td><td>35.10 Notes</td><td>(7) Items prohibited during programming and erasure
Do not perform the following operations during programming and erasure of the flash memory.</td><td>(7) Items prohibited during programming, erasure and blank checking
Do not perform the following operations during programming, erasure and blank checking of the flash memory.</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>53</td><td>2888</td><td>Electrical Characteristics</td><td>Table 39.33 RDC Conversion Performance (2/2)</td><td>Item | Condition | | Min. | Typ. | Max. | Unit
Response delay*4 | Electrical angle output response delay in fixed angular velocity | Angle conversion mode 0 | –0.2 | — | 0.20 | °/10000 min^{–1}
Angle conversion mode 1 | –0.2 | — | 0.20
BIST determination time*5 | Obtaining the sum of squares in amplitude abnormality detection BIST (L side) | — | — | 1 | ms
Obtaining the sum of squares in amplitude abnormality detection BIST (H side) | — | — | 1 | ms
ADBIST | — | — | 32 | µs
Angle conversion BIST (angle determination threshold is within ±8 LSB) | — | — | 10 | ms
Resolver signal error detection BIST | — | — | 0.5 | ms
Resolver signal cut off detection BIST | — | — | 1 | ms
Conversion error BIST | — | — | 10 | ms
Power short error BIST | — | — | 80 | µs
Ground short error BIST | — | — | 80 | µs
BIST recovery time*6 | All kinds of BIST | — | — | 10 | ms</td><td>Item | Condition | | Min. | Typ. | Max. | Unit
Response delay*4 | Electrical angle output response delay in fixed angular velocity | Angle conversion mode 0 | –0.2 | — | 0.20 | °/10000 min^{–1}
Angle conversion mode 1 | –0.2 | — | 0.20
BIST determination time*5 | Obtaining the sum of squares in amplitude abnormality detection BIST (L side) | — | — | 1 | ms
Obtaining the sum of squares in amplitude abnormality detection BIST (H side) | — | — | 1 | ms
ADBIST | — | — | 32 | µs
Angle conversion BIST (angle determination threshold is within ±16 LSB) | — | — | 10 | ms
Resolver signal error detection BIST | — | — | 0.5 | ms
Resolver signal cut off detection BIST | — | — | 1 | ms
Conversion error BIST | — | — | 10 | ms
Power short error BIST | — | — | 80 | µs
Ground short error BIST | — | — | 80 | µs
BIST recovery time*6 | All kinds of BIST | — | — | 10 | ms</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>54</td><td>461</td><td>CSIH</td><td>Table 11.25 CSIHnTX0W Register Contents (2/2)</td><td>29 | CSIHnEDL | Specifies whether the associated data requires the extended data length (EDL) option.
0: Normal operation
1: Enables the extended data length.
The associated data is transmitted as a 16-bit packet. No inter-data time or idle time will be inserted after the data is transmitted.
If CSIHnCTL1.CSIHnEDLE = 1 and CSIHnTX0W.CSIHnEDL = 1, the subsequent data must have the same CS selection. If CS is modified for the subsequent data, the correct operation is not assured.
CAUTION: This bit is only available if CSIHnCTL1.CSIHnEDLE = 1.
28 to 20 | Reserved | When read, the value after a reset is read. When writing, write the value after a reset.</td><td>29 | CSIHnEDL | Specifies whether the associated data requires the extended data length (EDL) option.
0: Normal operation
1: Enables the extended data length.
The associated data is transmitted as a 16-bit packet. No inter-data time or idle time will be inserted after the data is transmitted.
If CSIHnCTL1.CSIHnEDLE = 1 and CSIHnTX0W.CSIHnEDL = 1, the subsequent data must have the same CS selection. If CS is modified for the subsequent data, the correct operation is not assured.
CAUTION: This bit is only available if CSIHnCTL1.CSIHnEDLE = 1.
28 to 20 | Reserved | When read, the value after a reset is read. When writing, write the value after a reset.
Note that these bits should be written to 00FH when CSx (either x = 0 to 3) is used in master</td><td>Additional Description</td><td>TN-RH8-B0303A/E</td><td></td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>55</td><td>150</td><td>Pins</td><td>Table 2.61 C1M–A1 Pin Function (1/3)</td><td>
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>AnVREFH (n = 0 to 2)</td><td>—</td><td>ADCCn voltage supply and reference voltage</td></tr>
<tr><td>AnVSS (n = 0 to 2)</td><td>—</td><td>ADCCn ground</td></tr>
<tr><td>ADCCnTRG (n =0 to 2)</td><td>I</td><td>ADCCn trigger</td></tr>
<tr><td>ADCC0Ipq (p = 0 to 3, q = 0 to 3)
This excludes the combination of p = 2 and q = 2 or 3 and of p = 3 and q = 1 to 3.</td><td>I</td><td>ADCC0 input channel pq</td></tr>
<tr><td>ADCC1Ipq (p = 0 to 3, q = 0 to 3)
This excludes the combination of p = 3 and q = 0 or 3.</td><td>I</td><td>ADCC1 input channel pq</td></tr>
<tr><td>ADCC2Ipq (p = 1, q = 1 to 3)</td><td>I</td><td>ADCC2 input channel pq</td></tr>
</table>
</td><td>
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th></tr>
<tr><td>AnVREFH (n = 0 to 2)</td><td>—</td><td>ADCCn voltage supply and reference voltage</td></tr>
<tr><td>AnVSS (n = 0 to 2)</td><td>—</td><td>ADCCn ground</td></tr>
<tr><td>ADCCnTRG (n =0 to 2)</td><td>I</td><td>ADCCn trigger</td></tr>
<tr><td>ADCC0Ipq (p = 0 to 3, q = 0 to 3)
This excludes the combination of p = 2 and q = 2 or 3 and of p = 3 and q = 1 to 3.</td><td>I</td><td>ADCC0 input channel pq</td></tr>
<tr><td>ADCC1Ipq (p = 0 to 3, q = 0 to 3)
This excludes the combination of p = 3 and q = 0 or 3.</td><td>I</td><td>ADCC1 input channel pq</td></tr>
<tr><td>ADCC2Ipq (p = 0 to 1, q = 0 to 3)
This excludes the combination of p = 1 and q = 1 to 3.</td><td>I</td><td>ADCC2 input channel pq</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>56</td><td>1566</td><td>TAUJ</td><td>Table 19.64 Contents of TAUJnCMORm Register of Slave Channel for PWM Output Function</td><td>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>15, 14</td><td>TAUJnCKS[1:0]</td><td>These bits select the operation clock.
00: Prescaler output CK0
01: Prescaler output CK1
10: Prescaler output CK2
11: Prescaler output CK3
The value of the TAUJnCKS[1:0] bit of the master and slave channel(s) must be identical.</td></tr>
<tr><td>13, 12</td><td>TAUJnCCS[1:0]</td><td>00: Uses the operation clock as a counter clock.</td></tr>
<tr><td>11</td><td>TAUJnMAS</td><td>0: Channel is slave channel</td></tr>
<tr><td>10 to 8</td><td>TAUJnSTS[2:0]</td><td>100: INTTAUJnIm of master channel is a start trigger.</td></tr>
<tr><td>7, 6</td><td>TAUJnCOS[1:0]</td><td>00: Not used, so set to 00</td></tr>
<tr><td>5</td><td>Reserved</td><td>When read, the value after reset is read.
When writing, write the value after reset.</td></tr>
<tr><td>4 to 1</td><td>TAUJnMD[4:1]</td><td>0100: One-count mode</td></tr>
<tr><td>0</td><td>TAUJnMD0</td><td>1: INTTAUJnIm is generated at the start of operation.</td></tr>
</table>
</td><td>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Function</th></tr>
<tr><td>15, 14</td><td>TAUJnCKS[1:0]</td><td>These bits select the operation clock.
00: Prescaler output CK0
01: Prescaler output CK1
10: Prescaler output CK2
11: Prescaler output CK3
The value of the TAUJnCKS[1:0] bit of the master and slave channel(s) must be identical.</td></tr>
<tr><td>13, 12</td><td>TAUJnCCS[1:0]</td><td>00: Uses the operation clock as a counter clock.</td></tr>
<tr><td>11</td><td>TAUJnMAS</td><td>0: Channel is slave channel</td></tr>
<tr><td>10 to 8</td><td>TAUJnSTS[2:0]</td><td>100: INTTAUJnIm of master channel is a start trigger.</td></tr>
<tr><td>7, 6</td><td>TAUJnCOS[1:0]</td><td>00: Not used, so set to 00</td></tr>
<tr><td>5</td><td>Reserved</td><td>When read, the value after reset is read.
When writing, write the value after reset.</td></tr>
<tr><td>4 to 1</td><td>TAUJnMD[4:1]</td><td>0100: One-count mode</td></tr>
<tr><td>0</td><td>TAUJnMD0</td><td>1: INTTAUJnIm is not generated at the start of operation.</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>57</td><td>76</td><td>Overview</td><td>Table 1.5 Pin Assignments of RH850/C1M–A1 (2/4)</td><td>
<table>
<tr><th>Pin Number</th><th>Pin Name</th></tr>
<tr><td>45</td><td>A0VSS</td></tr>
<tr><td>46</td><td>ADCC0I30</td></tr>
<tr><td>47</td><td>A0VCC</td></tr>
<tr><td>48</td><td>P7_0/TAUD0I5/TAUD0O5/TAUJ0I0/TAUJ0O0/ADCC1TRG/CSIH2SC</td></tr>
<tr><td>49</td><td>P7_2/TAUD0I7/TAUD0O7/TAUJ0I2/TAUJ0O2/SCI0RXD/CSIH2SO</td></tr>
<tr><td>50</td><td>VDD</td></tr>
<tr><td>51</td><td>P7_4/TAUD0I8/TAUD0O8/TAUJ0I3/TAUJ0O3/SCI0TXD/CSIH2SI</td></tr>
<tr><td>52</td><td>VSS</td></tr>
<tr><td>53</td><td>P5_0/RLIN32RX/SCI0RXD/CSIH2CSS3</td></tr>
<tr><td>54</td><td>P5_1/RLIN32TX/SCI0TXD/CSIH2SSI</td></tr>
<tr><td>55</td><td>P5_2/RLIN31RX/SCI0SCK/SCI0SCK/CSIH2RYI/CSIH2RYO</td></tr>
<tr><td>56</td><td>P5_3/RLIN31TX/SCI1SCK/SCI1SCK</td></tr>
</table>
</td><td>
<table>
<tr><th>Pin Number</th><th>Pin Name</th></tr>
<tr><td>45</td><td>A0VSS</td></tr>
<tr><td>46</td><td>ADCC0I30</td></tr>
<tr><td>47</td><td>A0VCC</td></tr>
<tr><td>48</td><td>P7_0/TAUD0I5/TAUD0O5/TAUJ0I0/TAUJ0O0/ADCC1TRG/CSIH2SC</td></tr>
<tr><td>49</td><td>P7_2/TAUD0I7/TAUD0O7/TAUJ0I2/TAUJ0O2/SCI0RXD/CSIH2SO</td></tr>
<tr><td>50</td><td>VDD</td></tr>
<tr><td>51</td><td>P7_4/TAUD0I8/TAUD0O8/TAUJ0I3/TAUJ0O3/SCI0TXD/CSIH2SI</td></tr>
<tr><td>52</td><td>VSS</td></tr>
<tr><td>53</td><td>P5_0/RLIN32RX/SCI0RXD/CSIH2CSS3</td></tr>
<tr><td>54</td><td>P5_1/RLIN32TX/SCI0TXD/CSIH2SSI</td></tr>
<tr><td>55</td><td>P5_2/RLIN31RX/SCI0SCK/SCI0SCK/CSIH2RYI/CSIH2RYO</td></tr>
<tr><td>56</td><td>P5_3/RLIN31TX/SCI1SCK</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>58</td><td>2890</td><td>Electrical Characteristics</td><td>Table 39.35 Error Detect Characteristics</td><td>
<table>
<tr><td>R/D conversion error (over control declination) Recognition level for internal control declination (ε)*3</td><td>High side</td><td>00CA8H</td><td>*4</td></tr>
<tr><td></td><td>Low side</td><td>1FFF3H</td><td></td></tr>
</table>
</td><td>
<table>
<tr><td>R/D conversion error (over control declination) Recognition level for internal control declination (ε)*3</td><td>High side</td><td>00CA8H</td><td>*4</td></tr>
<tr><td></td><td>Low side</td><td>7F358H</td><td></td></tr>
</table>
</td><td>Description Change</td><td>TN-RH8-B0467A/E</td><td>–</td></tr>
<tr><td>59</td><td>2223</td><td>EMU3</td><td>Table 25.144 EMU3nNRECUk Register Contents (2/2)</td><td>Note: For details, see Section 25.4.7.3, Independent Rectangle IP2.</td><td>Note: For details, see Section 25.4.7.3, Independent Rectangle IP2.
CAUTION: When rewriting this register, be sure to follow steps (1) and (2) below.
This caution also applies to first-time writes.
(1) Write the following value in 32-bit access.
UMOD=0, UINT=0, UEN=0, UPTN=(set any value), UCMP=(set any value)
(2) UMOD, UINT, UEN, and UPTN settings should be written while retaining the values written in (1) of UCMP.</td><td>Description Change</td><td>TN-RH8-B0466A/E</td><td>–</td></tr>
<tr><td>60</td><td>2225</td><td>EMU3</td><td>Table 25.145 EMU3nNRECVk Register Contents (2/2)</td><td>Note: For details, see Section 25.4.7.3, Independent Rectangle IP2.</td><td>Note: For details, see Section 25.4.7.3, Independent Rectangle IP2.
CAUTION: When rewriting this register, be sure to follow steps (1) and (2) below.
This caution also applies to first-time writes.
(1) Write the following value in 32-bit access.
VMOD=0, VINT=0, VEN=0, VPTN=(set any value), VCMP=(set any value)
(2) VMOD, VINT, VEN, and VPTN settings should be written while retaining the values written in (1) of VCMP.</td><td>Description Change</td><td>TN-RH8-B0466A/E</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>61</td><td>2227</td><td>EMU3</td><td>Table 25.146 EMU3nNRECWk Register Contents (2/2)</td><td>Note: For details, see Section 25.4.7.3, Independent Rectangle IP2.</td><td>Note: For details, see Section 25.4.7.3, Independent Rectangle IP2.
CAUTION: When rewriting this register, be sure to follow steps (1) and (2) below.
This caution also applies to first-time writes.
(1) Write the following value in 32-bit access.
WMOD=0, WINT=0, WEN=0, WPTN=(set any value), WCMP=(set any value)
(2) WMOD, WINT, WEN, and WPTN settings should be written while retaining the values written in (1) of WCMP.</td><td>Description Change</td><td>TN-RH8-B0466A/E</td><td>–</td></tr>
<tr><td>62</td><td>1590</td><td>TSG3</td><td>Table 20.13 TSG3nCTL5 Register Contents (2/2)</td><td>none</td><td>CAUTION
TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.</td><td>Description Change</td><td>TN-RH8-B0468A/E</td><td>–</td></tr>
<tr><td>63</td><td>1592</td><td>TSG3</td><td>Table 20.14 TSG3nCTL6 Register Contents (2/2)</td><td>none</td><td>CAUTION
TSG3nATxx register bits should be set when the timer is stopped (TSG3nSTR0.TSG3nTE = 0).
Only the same value with current setting can be written during timer operation (TSG3nSTR0.TSG3nTE = 1).
If the different value is written to this register when TSG3nSTR0.TSG3nTE = 1,
timer operation cannot be guaranteed.</td><td>Description Change</td><td>TN-RH8-B0468A/E</td><td>–</td></tr>
<tr><td>64</td><td>2367</td><td>RDC3A</td><td>Table 26.23 RDC3AnSCCOR0 Register Contents</td><td>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>31 to 28</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>27 to 16</td><td>COSPO[11:0]</td><td>Cosine Phase Correction
Specifies the angular correction value for the phi to be input to the COS ROM table as a 12-bit singed integer.*1
b27-b16
000_H: 0° (no correction)
$7FF_H$: +180° (maximum correction in the positive direction)
800_H: – 180° (maximum correction in the negative direction)</td></tr>
<tr><td>15 to 12</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>11 to 0</td><td>SINPO[11:0]</td><td>Sine Phase Correction
Specifies the angular correction value for the phi to be input to the SIN ROM table as a 12-bit signed integer.*1
b11-b0
000_H: 0° (no correction)
$7FF_H$: +180° (maximum correction in the positive direction)
800_H: – 180° (maximum correction in the negative direction)</td></tr>
</table>
</td><td>
<table>
<tr><th>Bit Position</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>31 to 28</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>27 to 16</td><td>COSPO[11:0]</td><td>Cosine Angle Correction
Specifies the angular correction value for the phi to be input to the COS ROM table as a 12-bit singed integer.*1
b27-b16
000_H: 0° (no correction)
$7FF_H$: +180° (maximum correction in the positive direction)
800_H: – 180° (maximum correction in the negative direction)</td></tr>
<tr><td>15 to 12</td><td>Reserved</td><td>These bits are read as 0. The write value should be 0.</td></tr>
<tr><td>11 to 0</td><td>SINPO[11:0]</td><td>Sine Angle Correction
Specifies the angular correction value for the phi to be input to the SIN ROM table as a 12-bit signed integer.*1
b11-b0
000_H: 0° (no correction)
$7FF_H$: +180° (maximum correction in the positive direction)
800_H: – 180° (maximum correction in the negative direction)</td></tr>
</table>
</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>65</td><td>2429</td><td>RDC3A</td><td>26.4.2.5 Sine and Cosine Angle Correction Function</td><td>The RDC is capable of handling the mounting of the resolver at an angle to the motor shaft by correcting the resulting orthogonality errors of the sine and cosine signals from the resolver. Correction in this case is by adding fixed values for
correction to the phi angles to be input to the individual SINROM and COSROM tables. These values are set in the SINPO[11:0] and COSPO[11:0] bits in the sine and cosine angle correction register. Set these bits to 0° for angle conversion BIST.
Sine phase correction bits SINPO[11:0] = 000H
Cosine phase correction bits COSPO[11:0] = 000H</td><td>The RDC is capable of handling the mounting of the resolver at an angle to the motor shaft by correcting the resulting orthogonality errors of the sine and cosine signals from the resolver. Correction in this case is by adding fixed values for
correction to the phi angles to be input to the individual SINROM and COSROM tables. These values are set in the SINPO[11:0] and COSPO[11:0] bits in the sine and cosine angle correction register. Set these bits to 0° for angle conversion BIST.
Sine angle correction bits SINPO[11:0] = 000H
Cosine angle correction bits COSPO[11:0] = 000H</td><td>Writing Error</td><td>–</td><td>–</td></tr>
<tr><td>66</td><td>2439</td><td>RDC3A</td><td>26.4.5.1 Built-in Self-Test Function</td><td>(5) Set the phase correction bits in the sine and cosine angle correction register to 0° when executing the angle conversion BIST.
Sine phase correction bits SINPO[11:0] = 000H
Cosine phase correction bits COSPO[11:0] = 000H</td><td>(5) Set the phase correction bits in the sine and cosine angle correction register to 0° when executing the angle conversion BIST.
Sine angle correction bits SINPO[11:0] = 000H
Cosine angle correction bits COSPO[11:0] = 000H</td><td>Writing Error</td><td>–</td><td>–</td></tr>
</table>

<table>
<tr><th>No.</th><th>PDF page (Rev.1.20)</th><th>Section</th><th>Chapter title (Chart title)</th><th>Error</th><th>Correct</th><th>Change reason</th><th>Notice situation</th><th>Note</th></tr>
<tr><td>67</td><td>2816</td><td>Flash Memory</td><td>Table 35.4 Summary of Security Functions</td><td>
<table>
<tr><th>Function</th><th>Description</th></tr>
<tr><td>OTP</td><td>OTP can be individually set for each block of the user area and the user boot area of code flash memory. When the OTP setting is made for an area, programming by serial programming and by self-programming is prohibited. Once set, the OTP setting cannot be released. Furthermore, since execution of the configuration clearing command is prohibited for any area for which OTP has been set, changing a security setting from "prohibited" to "permitted" is not possible.</td></tr>
<tr><td>ID authentication</td><td>The result of ID authentication can be used to control the connection of a dedicated flash memory programmer for serial programming. The result of ID authentication can also be used to control enabling of programming of the code flash memory by self-programming.</td></tr>
<tr><td>Prohibition of connection of a dedicated flash memory programmer</td><td>The connection of a dedicated flash memory programmer for serial programming is prohibited. Since execution of the configuration clearing command is also prohibited when the connection of a dedicated flash memory programmer is prohibited, changing a security setting from "prohibited" to "permitted" is not possible.</td></tr>
<tr><td>Prohibition of block erasure commands</td><td>Block erasure commands at the time of serial programming are prohibited. Since execution of the configuration clearing command is also prohibited when block erasure commands are prohibited, changing a security setting from "prohibited" to "permitted" is not possible.</td></tr>
<tr><td>Prohibition of programming commands</td><td>Block erasure commands and programming commands at the time of serial programming are prohibited. Block erasure commands can be run only by the method of erasing all user areas from Block 0 in turn → erasing the user boot areas → erasing all data areas from Block 0 in turn.
Only through execution of the configuration clearing command, the prohibition can be lifted.</td></tr>
<tr><td>Prohibition of read commands</td><td>Read commands at the time of serial programming are prohibited. Only through execution of the configuration clearing command, the prohibition can be lifted.</td></tr>
</table>
</td><td>
<table>
<tr><th>Function</th><th>Description</th></tr>
<tr><td>OTP</td><td>OTP can be individually set for each block of the user area and the user boot area of code flash memory. When the OTP setting is made for an area, programming by serial programming and by self-programming is prohibited. Once set, the OTP setting cannot be released. Furthermore, since execution of the configuration clearing command is prohibited for any area for which OTP has been set, changing a security setting from "prohibited" to "permitted" is not possible.</td></tr>
<tr><td>ID authentication</td><td>The result of ID authentication can be used to control the connection of a dedicated flash memory programmer for serial programming. The result of ID authentication can also be used to control enabling of programming of the code flash memory by self-programming.</td></tr>
<tr><td>Prohibition of connection of a dedicated flash memory programmer *1</td><td>The connection of a dedicated flash memory programmer for serial programming is prohibited. Since execution of the configuration clearing command is also prohibited when the connection of a dedicated flash memory programmer is prohibited, changing a security setting from "prohibited" to "permitted" is not possible.</td></tr>
<tr><td>Prohibition of block erasure commands *2</td><td>Block erasure commands at the time of serial programming are prohibited. Since execution of the configuration clearing command is also prohibited when block erasure commands are prohibited, changing a security setting from "prohibited" to "permitted" is not possible.</td></tr>
<tr><td>Prohibition of programming commands *2</td><td>Block erasure commands and programming commands at the time of serial programming are prohibited. Block erasure commands can be run only by the method of erasing all user areas from Block 0 in turn → erasing the user boot areas → erasing all data areas from Block 0 in turn.
Only through execution of the configuration clearing command, the prohibition can be lifted.</td></tr>
<tr><td>Prohibition of read commands *2</td><td>Read commands at the time of serial programming are prohibited. Only through execution of the configuration clearing command, the prohibition can be lifted.</td></tr>
</table>
Note1. The "Prohibition of connection of a dedicated flash memory programmer" function can be used in conjunction with "ID authentication" or the prohibition of commands (*2).
Note2. Prohibition of commands (for block erasure, programming, and reading) can be set independently.
</td><td>Description Change</td><td>TN-RH8-BxxxxA/E</td><td>–</td></tr>
<tr><td>68</td><td>2838</td><td>Flash Security</td><td>36.1.1.2 Functions Unique to Serial Programming Mode</td><td>Three functions are provided as security functions unique to serial programming mode: ID authentication, prohibition of programming, erasure, and read commands, and prohibition of serial programmer connection. Parallel use of these functions is not allowed.</td><td>Three functions are provided as security functions unique to serial programming mode: ID authentication, prohibition of programming, erasure, and read commands, and prohibition of serial programmer connection.</td><td>Description Change</td><td>TN-RH8-BxxxxA/E</td><td>–</td></tr>
<tr><td>69</td><td>2838</td><td>Flash Security</td><td>Table 36.1 Security Functions in Each Mode</td><td>
<table>
<tr><th>Operation Mode</th><th>Code Flash and Data Flash, ID Code Protection</th><th>Restriction on Debug Interface Connection</th></tr>
<tr><td>User boot mode</td><td>• SELF ID authentication
• OTP (parallel use possible)</td><td>• Security level 1 (OCD ID authentication)
• Security level 2 (Debug interface connection is prohibited)</td></tr>
<tr><td>Serial programming mode</td><td>• ID authentication
• Programming commands, block erasure commands, and read commands are prohibited.
• Connection of serial programmers is prohibited. (The above three cannot be used in parallel.)
• OTP (parallel use possible)</td><td>• No function (Debug interface connection is always prohibited.)</td></tr>
</table>
</td><td>
<table>
<tr><th>Operation Mode</th><th>Code Flash and Data Flash, ID Code Protection</th><th>Restriction on Debug Interface Connection</th></tr>
<tr><td>User boot mode</td><td>• SELF ID authentication
• OTP (parallel use possible)</td><td>• Security level 1 (OCD ID authentication)
• Security level 2 (Debug interface connection is prohibited)</td></tr>
<tr><td>Serial programming mode</td><td>• ID authentication
• Programming commands, block erasure commands, and read commands are prohibited.
• Connection of serial programmers is prohibited.
• OTP (parallel use possible)</td><td>• No function (Debug interface connection is always prohibited.)</td></tr>
</table>
</td><td>Description Change</td><td>TN-RH8-BxxxxA/E</td><td>–</td></tr>
<tr><td>70</td><td>2414</td><td>RDC3A</td><td>26.4.1.4 Required Sensor Selection Function</td><td>The DC resolver signal (E・sin θ, E・cos θ) which does not contain excitation component can be used by setting the SENS bit in the RDC3AnREF register to 0. When the DC resolver signal is used, the excitation component extraction function is disabled.</td><td>The DC resolver signal (E・sin θ, E・cos θ) which does not contain excitation component can be used by setting the SENS bit in the RDC3AnREF register to 0. When the DC resolver signal is used, the excitation signal outputs(RDC3AnRSO, RDC3AnCOM) and the excitation component extraction function are disabled.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
<tr><td>71</td><td>2430</td><td>RDC3A</td><td>26.4.3.1 Excitation Signal Output (RDC3AnRSO, RDC3AnCOM)</td><td>The amplitude of the sine wave signal that is output from the RDC3AnRSO pin is set in the EXOC[1:0] bits in the RDC3AnATMNT0 register. The amplitude of the standard value is 0.4 × RVCC [Vp–p].</td><td>The amplitude of the sine wave signal that is output from the RDC3AnRSO pin is set in the EXOC[1:0] bits in the RDC3AnATMNT0 register. The amplitude of the standard value is 0.4 × RVCC [Vp–p].
When operation with a DC resolver is selected (by setting the combination of values as EXIO = 1 and SENS = 0), the excitation signal outputs(RDC3AnRSO, RDC3AnCOM) are disabled.</td><td>Additional Description</td><td>–</td><td>–</td></tr>
</table>

End of the list