

# RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan  
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RH8-B0573B/E	Rev.	2.00
Title	RH850 DNF Pulse width description		Information Category	Technical Notification		
Applicable Product	RH850/F1x RH850/P1x-C, P1L-C RH850/U2Ax	Lot No.	Reference Document	See related documents below.		
		All lot				

## [Overview]

The description of the pulse width calculation formula of the DNF (digital noise filter) is incorrect.

## [Reference Documents]

Group	Document Title	Rev.	Document Number
F1L	RH850/F1L Group User's Manual: Hardware	1.33	R01UH0390EJ0133
F1H	RH850/F1H Group User's Manual: Hardware	1.12	R01UH0445EJ0112
F1H	RH850/F1H PREMIUM 100pin Version User's Manual: Hardware	1.00	R01UH0631EJ0100
F1M	RH850/F1M Group User's Manual: Hardware	1.03	R01UH0518EJ0103
F1K	RH850/F1K Group User's Manual: Hardware	1.10	R01UH0562EJ0110
F1KH, F1KM	RH850/F1KH, RH850/F1KM User's Manual: Hardware	1.30	R01UH0684EJ0130
P1x-C	RH850/P1x-C Group User's Manual: Hardware	1.40	R01UH0517EJ0140
P1L-C	RH850/P1L-C Group User's Manual: Hardware	1.20	R01UH0592EJ0120
U2Ax	RH850/U2A-EVA Group User's Manual: Hardware	1.50	R01UH0864EJ0150

## [Change point]

The following description will be changed in the User's Manual (Red character)

See below.

- (1) RH850/F1L
- (2) RH850/F1H
- (3) RH850/F1H PREMIUM
- (4) RH850/F1M
- (5) RH850/F1K
- (6) RH850/F1KH, F1KM
- (7) RH850/ P1x-C
- (8) RH850/ P1L-C
- (9) RH850/ U2Ax

(1) RH850/F1L, (2) RH850/F1H, (3) RH850/F1H PREMINUM, (4) RH850/F1M, (5) RH850/F1K

Section 2 Pin Functions

**2.13.3 Digital filters**

**2.13.3.1 Digital filter characteristic**

<Before>

DNFA<name>CTL.DNFA<name>NFSTS[1:0] determines the number of same level samples (2 to 5):

$$s = \text{DNFA<name>NFSTS}[1:0] + 2$$

External signal pulse shorter than the following are suppressed at all times.

$$s \times 1/fs$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$(s + 1) \times 1/fs$$

External signal pulses in the following range may be suppressed or judged as valid.

$$s \times 1/fs \text{ to } (s + 1) \times 1/fs$$

The filter operation is illustrated in the figure below with DNFA<name>NFSTS[1:0] = 01B, i.e. s = 3 same level samples.

<After>

DNFA<name>CTL.DNFA<name>NFSTS[1:0] determines the number of same level samples (2 to 5):

$$s = \text{DNFA<name>NFSTS}[1:0] + 2$$

External signal pulse shorter than the following are suppressed at all times.

$$(s - 1) \times 1/fs$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$s \times 1/fs$$

External signal pulses in the following range may be suppressed or judged as valid.

$$(s - 1) \times 1/fs \text{ to } s \times 1/fs$$

The filter operation is illustrated in the figure below with DNFA<name>NFSTS[1:0] = 01B, i.e. s = 3 same level samples.

(6) RH850/F1KH, F1KM

Section 2A Pin Function of RH850/F1KH-D8

**2A.13.3 Digital filters**

**2A.13.3.1 Digital filter characteristic**

Section 2B Pin Function of RH850/F1KM-S4, RH850/F1KM-S2

**2B.13.3 Digital filters**

**2B.13.3.1 Digital filter characteristic**

Section 2C Pin Function of RH850/F1KM-S1

**2C.13.3 Digital filters**

**2C.13.3.1 Digital filter characteristic**

<Before>

DNFA<name>CTL.DNFA<name>NFSTS[1:0] determines the number of same level samples, “s”, (2 to 5):

$$s = \text{DNFA}\langle\text{name}\rangle\text{NFSTS}[1:0] + 2$$

External signal pulses shorter than the following are suppressed at all times.

$$s \times 1/\text{fs}$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$(s + 1) \times 1/\text{fs}$$

External signal pulses in the following range may be suppressed or judged as valid.

$$s \times 1/\text{fs} \text{ to } (s + 1) \times 1/\text{fs}$$

The filter operation is illustrated in the figure below with DNFA<name>NFSTS[1:0] = 01B, i.e. s = 3 same level samples.

<After>

DNFA<name>CTL.DNFA<name>NFSTS[1:0] determines the number of same level samples, “s”, (2 to 5):

$$s = \text{DNFA}\langle\text{name}\rangle\text{NFSTS}[1:0] + 2$$

External signal pulses shorter than the following are suppressed at all times.

$$(s - 1) \times 1/\text{fs}$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$s \times 1/\text{fs}$$

External signal pulses in the following range may be suppressed or judged as valid.

$$(s - 1) \times 1/\text{fs} \text{ to } s \times 1/\text{fs}$$

The filter operation is illustrated in the figure below with DNFA<name>NFSTS[1:0] = 01B, i.e. s = 3 same level samples.

(7) RH850/ P1x-C

## Section 2 Pin Functions

### 2.7.3.2 Digital filters

#### Digital filter characteristic

##### <Before>

DNFAnCTL.DNFAnNFSTS[1:0] determines the number  $s$  of same level samples (2 to 5):

External signal pulses, shorter than

$$\text{DNFAnNFSTS}[1:0] \times 1/\text{fs}$$

are always suppressed.

External signal pulses, longer than

$$(\text{DNFAnNFSTS}[1:0] + 1) \times 1/\text{fs}$$

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

$$\text{DNFAnNFSTS}[1:0] \times 1/\text{fs} \text{ to } (\text{DNFAnNFSTS}[1:0] + 1) \times 1/\text{fs}$$

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e.  $s = 3$  same level samples.

##### <After>

DNFAnCTL.DNFAnNFSTS[1:0] determines the number  $s$  of same level samples (2 to 5):

External signal pulses, shorter than

$$(\text{DNFAnNFSTS}[1:0] - 1) \times 1/\text{fs}$$

are always suppressed.

External signal pulses, longer than

$$\text{DNFAnNFSTS}[1:0] \times 1/\text{fs}$$

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

$$(\text{DNFAnNFSTS}[1:0] - 1) \times 1/\text{fs} \text{ to } \text{DNFAnNFSTS}[1:0] \times 1/\text{fs}$$

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e.  $s = 3$  same level samples.

(8) RH850/ P1L-C

## Section 2 Pin Functions

### 2.7.3.2 Digital filters

#### Digital filter characteristic

##### <Before>

DNFAnCTL.DNFAnNFSTS[1:0] determines the number  $s$  of same level samples (2 to 5):

External signal pulses, shorter than

$$\text{DNFAnNFSTS}[1:0] \times 1/\text{fs}$$

are always suppressed.

External signal pulses, longer than

$$(\text{DNFAnNFSTS}[1:0] + 1) \times 1/\text{fs}$$

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

$$\text{DNFAnNFSTS}[1:0] \times 1/\text{fs} \text{ to } (\text{DNFAnNFSTS}[1:0] + 1) \times 1/\text{fs}$$

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e.  $s = 3$  same level samples.

##### < After >

DNFAnCTL.DNFAnNFSTS[1:0] determines the number  $s$  of same level samples (2 to 5):

External signal pulses, shorter than

$$(\text{DNFAnNFSTS}[1:0] - 1) \times 1/\text{fs}$$

are always suppressed.

External signal pulses, longer than

$$\text{DNFAnNFSTS}[1:0] \times 1/\text{fs}$$

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

$$(\text{DNFAnNFSTS}[1:0] - 1) \times 1/\text{fs} \text{ to } \text{DNFAnNFSTS}[1:0] \times 1/\text{fs}$$

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e.  $s = 3$  same level samples.

(9) RH850/ U2Ax

## Section 2 Pin Function

### 2.7.2.2 Digital Filters (1) Digital Filter Characteristic

<Before>

External signal pulses shorter than the following are always suppressed.

$$s \times 1/f_s$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$(s + 1) \times 1/f_s$$

External signal pulses in the following range may be suppressed or judged as valid.

$$s \times 1/f_s \text{ to } (s + 1) \times 1/f_s$$

<After>

External signal pulses shorter than the following are always suppressed.

$$(s - 1) \times 1/f_s$$

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

$$s \times 1/f_s$$

External signal pulses in the following range may be suppressed or judged as valid.

$$(s - 1) \times 1/f_s \text{ to } s \times 1/f_s$$

Section 55 Electrical Characteristics

55.3.6.2 Interrupt, Wake-up and Error Input Timing

Table 55.37 Interrupt Timing

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t <sub>WNIH</sub>	*3	600			ns
		*4	20			μs
NMI input low level width	t <sub>WNIL</sub>	*3	600			ns
		*4	20			μs
NMI pulse rejection width*2	t <sub>WNIRJ</sub>		100		600	ns
INTPn input high level width	t <sub>WITH</sub>	*3	600			ns
		*4	20			μs
INTPn input low level width	t <sub>WITL</sub>	*3	600			ns
		*4	20			μs
INTPn pulse rejection width*2	t <sub>WIRJ</sub>		100		600	ns
RLIN3nRX wake-up input high level width	t <sub>WRLINH</sub>		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up input low level width	t <sub>WRLINL</sub>		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	t <sub>WRLINRJ</sub>		(S - 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
CANnRX wake-up input high level width	t <sub>WCANH</sub>		(S + 1) x 1/fs*1			ns
CANnRX wake-up input low level width	t <sub>WCANL</sub>		(S + 1) x 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t <sub>WCANRJ</sub>		(S - 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
FLXnRXDA wake-up input high level width	t <sub>WFLXH</sub>		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up input low level width	t <sub>WFLXL</sub>		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t <sub>WFLXRJ</sub>		(S - 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
ERRORINn wake-up input high level width	t <sub>WERRH</sub>		(S + 1) x 1/fs*1			ns
ERRORINn wake-up input low level width	t <sub>WERRL</sub>		(S + 1) x 1/fs*1			ns
ERRORINn wake-up pulse rejection width*2	t <sub>WERRRJ</sub>		(S - 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times  
fs: The value given by following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLK\_LSB  
PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA\_LPS is operated by CLK\_HSIOSC/20)

Note 4. Level Detection (CLKA\_LPS is operated by CLK\_LSIOSC)

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t <sub>WNIH</sub>	*3	600			ns
		*4	20			μs
NMI input low level width	t <sub>WNIL</sub>	*3	600			ns
		*4	20			μs
NMI pulse rejection width*2	t <sub>WNIRJ</sub>		100		600	ns
INTPn input high level width	t <sub>WITH</sub>	*3	600			ns
		*4	20			μs
INTPn input low level width	t <sub>WITL</sub>	*3	600			ns
		*4	20			μs
INTPn pulse rejection width*2	t <sub>WIRJ</sub>		100		600	ns
RLIN3nRX wake-up input high level width	t <sub>WRLINH</sub>		S x 1/fs*1			ns
RLIN3nRX wake-up input low level width	t <sub>WRLINL</sub>		S x 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	t <sub>WRLINRJ</sub>		(S - 1) x 1/fs*1		S x 1/fs*1	ns
CANnRX wake-up input high level width	t <sub>WCANH</sub>		S x 1/fs*1			ns
CANnRX wake-up input low level width	t <sub>WCANL</sub>		S x 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t <sub>WCANRJ</sub>		(S - 1) x 1/fs*1		S x 1/fs*1	ns
FLXnRXDA wake-up input high level width	t <sub>WFLXH</sub>		S x 1/fs*1			ns
FLXnRXDA wake-up input low level width	t <sub>WFLXL</sub>		S x 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t <sub>WFLXRJ</sub>		(S - 1) x 1/fs*1		S x 1/fs*1	ns
ERRORINn wake-up input high level width	t <sub>WERRH</sub>		S x 1/fs*1			ns
ERRORINn wake-up input low level width	t <sub>WERRL</sub>		S x 1/fs*1			ns
ERRORINn wake-up pulse rejection width*2	t <sub>WERRRJ</sub>		(S - 1) x 1/fs*1		S x 1/fs*1	ns

Note 1. S: Number of sampling times  
fs: The value given by following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLK\_LSB  
PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA\_LPS is operated by CLK\_HSIOOSC/20)

Note 4. Level Detection (CLKA\_LPS is operated by CLK\_LSIOOSC)

55.3.6.4 ADTRG Timing

Table 55.39 ADCJnTRGm Timing

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCJnTRGm input high level width	t <sub>WADH</sub>		(S + 1) x 1/fs* <sup>1</sup>			ns
ADCJnTRGm input low level width	t <sub>WADL</sub>		(S + 1) x 1/fs* <sup>1</sup>			ns
ADCJnTRGm pulse rejection width* <sup>2</sup>	t <sub>WADRJ</sub>		(S - 1) x 1/fs* <sup>1</sup>		(S + 1) x 1/fs* <sup>1</sup>	ns

Note 1. S: Number of sampling times  
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLK\_ADC, CLKA\_ADC  
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCJnTRGm input high level width	t <sub>WADH</sub>		S x 1/fs* <sup>1</sup>			ns
ADCJnTRGm input low level width	t <sub>WADL</sub>		S x 1/fs* <sup>1</sup>			ns
ADCJnTRGm pulse rejection width* <sup>2</sup>	t <sub>WADRJ</sub>		(S - 1) x 1/fs* <sup>1</sup>		S x 1/fs* <sup>1</sup>	ns

Note 1. S: Number of sampling times  
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLK\_ADC, CLKA\_ADC  
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

55.3.6.5 Communication Signal Timing

Table 55.40 Control Signal

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	t <sub>WSENTIH</sub>	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs* <sup>1</sup>			ns
SENTnRX input low level width	t <sub>WSENTIL</sub>	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs* <sup>1</sup>			ns
SENTnRX pulse rejection width	t <sub>WSENTIRJ</sub>	Analog filter	100		600	ns
		Digital filter	(S - 1) x 1/fs* <sup>1</sup>		(S + 1) x 1/fs* <sup>1</sup>	ns
PSI5nRX input high level width* <sup>2</sup>	t <sub>WPSI5IH</sub>	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs* <sup>1</sup>			ns
PSI5nRX input low level width	t <sub>WPSI5IL</sub>	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs* <sup>1</sup>			ns
PSI5nRX pulse rejection width* <sup>2</sup>	t <sub>WPSI5IRJ</sub>	Analog filter	100		600	ns
		Digital filter	(S - 1) x 1/fs* <sup>1</sup>		(S + 1) x 1/fs* <sup>1</sup>	ns

Note 1. S: Number of sampling times  
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLK\_HSB  
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	t <sub>WSENTIH</sub>	Analog filter	600			ns
		Digital filter	S x 1/fs <sup>*1</sup>			ns
SENTnRX input low level width	t <sub>WSENTIL</sub>	Analog filter	600			ns
		Digital filter	S x 1/fs <sup>*1</sup>			ns
SENTnRX pulse rejection width	t <sub>WSENTIRJ</sub>	Analog filter	100		600	ns
		Digital filter	(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns
PSI5nRX input high level width <sup>*2</sup>	t <sub>WPSI5IH</sub>	Analog filter	600			ns
		Digital filter	S x 1/fs <sup>*1</sup>			ns
PSI5nRX input low level width	t <sub>WPSI5IL</sub>	Analog filter	600			ns
		Digital filter	S x 1/fs <sup>*1</sup>			ns
PSI5nRX pulse rejection width <sup>*2</sup>	t <sub>WPSI5IRJ</sub>	Analog filter	100		600	ns
		Digital filter	(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns

Note 1. S: Number of sampling times  
 fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLK\_HSB  
 PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

55.3.22 Timer Timing

Table 55.75 Timer Input Timing

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t <sub>WTDIH</sub>		(S + 1) x 1/fs <sup>*1</sup>			ns
TAUDnIm input low level width	t <sub>WTDIL</sub>		(S + 1) x 1/fs <sup>*1</sup>			ns
TAUDnIm pulse rejection width <sup>*2</sup>	t <sub>WTDRJ</sub>		(S - 1) x 1/fs <sup>*1</sup>		(S + 1) x 1/fs <sup>*1</sup>	ns
TAUJnIm input high level width	t <sub>WTJIH</sub>	Analog noise filter	600 <sup>*3</sup>			ns
		Digital noise filter	(S + 1) x 1/fs <sup>*1</sup>			ns
TAUJnIm input low level width	t <sub>WTJIL</sub>	Analog noise filter	600 <sup>*3</sup>			ns
		Digital noise filter	(S + 1) x 1/fs <sup>*1</sup>			ns
TAUJnIm pulse rejection width <sup>*2</sup>	t <sub>WTJRJ</sub>	Analog noise filter	100		600 <sup>*3</sup>	ns
		Digital noise filter	(S - 1) x 1/fs <sup>*1</sup>		(S + 1) x 1/fs <sup>*1</sup>	ns
TAPAnESO input high level width <sup>*4</sup>	t <sub>WTPIH</sub>	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs <sup>*1</sup>			ns
TAPAnESO input low level width <sup>*4</sup>	t <sub>WTPIL</sub>	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs <sup>*1</sup>			ns
TAPAnESO pulse rejection width <sup>*2, *4</sup>	t <sub>WTPRJ</sub>	Analog noise filter	100		600	ns
		Digital noise filter	(S - 1) x 1/fs <sup>*1</sup>		(S + 1) x 1/fs <sup>*1</sup>	ns
ENCAnTINm input high level width	t <sub>WENIH</sub>		(S + 1) x 1/fs <sup>*1</sup>			ns
ENCAnTINm input low level width	t <sub>WENIL</sub>		(S + 1) x 1/fs <sup>*1</sup>			ns
ENCAnTINm pulse rejection width <sup>*2</sup>	t <sub>WENRJ</sub>		(S - 1) x 1/fs <sup>*1</sup>		(S + 1) x 1/fs <sup>*1</sup>	ns
TSG3nPTSI <sub>m</sub> /ENCAnEx, TSG3nCLKI high level width	t <sub>WTGIH</sub>		(S + 1) x 1/fs <sup>*1</sup>			ns
TSG3nPTSI <sub>m</sub> /ENCAnEx, TSG3nCLKI low level width	t <sub>WTGIL</sub>		(S + 1) x 1/fs <sup>*1</sup>			ns
TSG3nPTSI <sub>m</sub> /ENCAnEx, TSG3nCLKI pulse rejection width <sup>*2</sup>	t <sub>WTGRJ</sub>		(S - 1) x 1/fs <sup>*1</sup>		(S + 1) x 1/fs <sup>*1</sup>	ns

Note 1. S: Number of sampling times  
fs: The value given by the following formula

$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLKA\_TAUJ (for TAUJ2 and TAUJ3), CLK\_HSB (others)  
PRS: 1, 2, 4, 8, ... , 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not).  
This characteristic is not tested in production.

Note 3. When CLK\_LSIO<sub>SC</sub> is selected by CLKA\_TAUJ register, at least one clock period of CLK\_LSIO<sub>SC</sub> (4.6 μs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 μs width may be rejected.

Note 4. By-pass of filter is possible. For details, see Section 2.7.2.10, ANF/DNF Type F1.

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t <sub>WTDIH</sub>		S x 1/fs <sup>*1</sup>			ns
TAUDnIm input low level width	t <sub>WTDIL</sub>		S x 1/fs <sup>*1</sup>			ns
TAUDnIm pulse rejection width <sup>*2</sup>	t <sub>WDRJ</sub>		(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns
TAUJnIm input high level width	t <sub>WTJIH</sub>	Analog noise filter	600 <sup>*3</sup>			ns
		Digital noise filter	S x 1/fs <sup>*1</sup>			ns
TAUJnIm input low level width	t <sub>WTJIL</sub>	Analog noise filter	600 <sup>*3</sup>			ns
		Digital noise filter	S x 1/fs <sup>*1</sup>			ns
TAUJnIm pulse rejection width <sup>*2</sup>	t <sub>WTJRJ</sub>	Analog noise filter	100		600 <sup>*3</sup>	ns
		Digital noise filter	(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns
TAPAnESO input high level width <sup>*4</sup>	t <sub>WTPIH</sub>	Analog noise filter	600			ns
		Digital noise filter	S x 1/fs <sup>*1</sup>			ns
TAPAnESO input low level width <sup>*4</sup>	t <sub>WTPIL</sub>	Analog noise filter	600			ns
		Digital noise filter	S x 1/fs <sup>*1</sup>			ns
TAPAnESO pulse rejection width <sup>*2, *4</sup>	t <sub>WTPRJ</sub>	Analog noise filter	100		600	ns
		Digital noise filter	(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns
ENCAnTINm input high level width	t <sub>WENIH</sub>		S x 1/fs <sup>*1</sup>			ns
ENCAnTINm input low level width	t <sub>WENIL</sub>		S x 1/fs <sup>*1</sup>			ns
ENCAnTINm pulse rejection width <sup>*2</sup>	t <sub>WENRJ</sub>		(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns
TSG3nPTSI <sub>m</sub> /ENCAnEx, TSG3nCLKI high level width	t <sub>WTGIH</sub>		S x 1/fs <sup>*1</sup>			ns
TSG3nPTSI <sub>m</sub> /ENCAnEx, TSG3nCLKI low level width	t <sub>WTGIL</sub>		S x 1/fs <sup>*1</sup>			ns
TSG3nPTSI <sub>m</sub> /ENCAnEx, TSG3nCLKI pulse rejection width <sup>*2</sup>	t <sub>WTGRJ</sub>		(S - 1) x 1/fs <sup>*1</sup>		S x 1/fs <sup>*1</sup>	ns

Note 1. S: Number of sampling times  
fs: The value given by the following formula

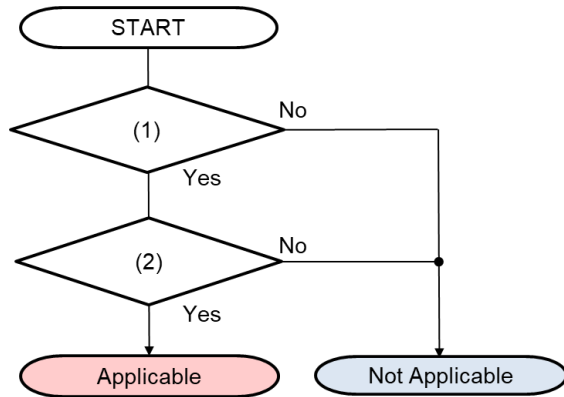
$$f_s = \frac{f_{DNFCK}}{PRS}$$

f<sub>DNFCK</sub>: frequency of CLKA\_TAUJ (for TAUJ2 and TAUJ3), CLK\_HSB (others)  
PRS: 1, 2, 4, 8, ... , 128

- Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not). This characteristic is not tested in production.
- Note 3. When CLK\_LSIOSC is selected by CLKA\_TAUJ register, at least one clock period of CLK\_LSIOSC (4.6 μs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 μs width may be rejected.
- Note 4. By-pass of filter is possible. For details, see Section 2.7.2.10, ANF/DNF Type F1.

[Judgement Flow]

(1)	Is the DNF used?
(2)	Does the calculation of suppressed pulse width and passed pulse width using the formula?



END