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RENESAS TECHNICAL UPDATE

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製品分類	MPU & MCU	発行番号	TN-RH8-B0573B/J	Rev.	第2版
題名	RH850 DNF パルス幅の記載誤り		情報分類	技術情報	
適用製品	RH850/F1x RH850/P1x-C, P1L-C RH850/U2Ax	対象ロット等 全て	関連資料	下記の関連文書を参照	

RH850/RH850/F1x, RH850/P1x-C, P1L-C, RH850/U2Ax シリーズのユーザーズマニュアルにおいて、デジタルノイズフィルタ特性の記載に誤りがあることが判明しましたので報告致します。

1. 概要

DNF (デジタルノイズフィルタ)のパルス幅計算式の記述が誤っています。

2. 参照文書

Group	Document Title	Rev.	Document Number
F1L	RH850/F1L ユーザーズマニュアル ハードウェア編	1.33	R01UH0390JJ0133
F1H	RH850/F1H ユーザーズマニュアル ハードウェア編	1.12	R01UH0445JJ0112
F1H	RH850/F1H PREMIUM 100pin版 ユーザーズマニュアル ハードウェア編	1.01	R01UH0631JJ0101
F1M	RH850/F1M ユーザーズマニュアル ハードウェア編	1.03	R01UH0518JJ0103
F1K	RH850/F1K ユーザーズマニュアル ハードウェア編	1.10	R01UH0562JJ0110
F1KH, F1KM	RH850/F1KH,RH850/F1KM ユーザーズマニュアル ハードウェア編	1.30	R01UH0684JJ0130
P1x-C	RH850/P1x-C Group User's Manual: Hardware	1.40	R01UH0517EJ0140
P1L-C	RH850/P1L-C Group User's Manual: Hardware	1.20	R01UH0592EJ0120
U2Ax	RH850/U2A-EVA Group User's Manual: Hardware	1.50	R01UH0864EJ0150

3. 変更箇所

ユーザーズマニュアルの以下の記述が変更されます。

(1) RH850/F1L

(2) RH850/F1H

(3) RH850/F1H PREMINUM

(4) RH850/F1M

(5) RH850/F1K

(6) RH850/F1KH, F1KM

(7) RH850/ P1x-C

(8) RH850/ P1L-C

(9) RH850/ U2Ax

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(1) RH850/F1L, (2) RH850/F1H, (3) RH850/F1H PREMINUM, (4) RH850/F1M, (5) RH850/F1K,

第２章 端子

2.13.3 デジタルフィルタ

2.13.3.1 デジタルフィルタ特性

<変更前>

DNFA<name>CTL.DNFA<name>NFSTS[1:0] で同レベルのサンプル数（2 ～ 5）を指定します。

s = DNFA<name>NFSTS[1:0] + 2

以下よりも短い外部信号パルスは常に抑制されます。

s × 1/fs

以下よりも長い外部信号パルスは常に有効と判断され、フィルタ出力へ送られます。

(s + 1) × 1/fs

以下の範囲内の外部信号パルスは抑制される場合もあれば、有効と判断される場合もあります。

s × 1/fs ～ (s + 1) × 1/fs

DNFA<name>NFSTS[1:0] = 01B (同レベルのサンプル数：3) としたときのフィルタ動作例を

次の図に示します。

<変更後>

DNFA<name>CTL.DNFA<name>NFSTS[1:0] で同レベルのサンプル数（2 ～ 5）を指定します。

s = DNFA<name>NFSTS[1:0] + 2

以下よりも短い外部信号パルスは常に抑制されます。

(s – 1) × 1/fs

以下よりも長い外部信号パルスは常に有効と判断され、フィルタ出力へ送られます。

s × 1/fs

以下の範囲内の外部信号パルスは抑制される場合もあれば、有効と判断される場合もあります。

(s – 1) × 1/fs ～ s × 1/fs

DNFA<name>NFSTS[1:0] = 01B (同レベルのサンプル数：3) としたときのフィルタ動作例を

次の図に示します。

(6)　RH850/F1KH, F1KM

第 2A RH850/F1KH-D8 の端子

2A.13.3 デジタルフィルタ

2A.13.3.1 デジタルフィルタ特性

第 2B RH850/F1KM-S4, RH850/F1KM-S2 の端子

2B.13.3 デジタルフィルタ

2B.13.3.1 デジタルフィルタ特性

第 2C RH850/F1KM-S1 の端子

2C.13.3 デジタルフィルタ

2C.13.3.1 デジタルフィルタ特性

<変更前>

DNFA<*name*>CTL.DNFA<*name*>NFSTS[1:0]で同レベルのサンプル数（2～5）を指定します。

s＝DNFA<*name*>NFSTS[1:0] + 2

以下よりも短い外部信号パルスは常に抑制されます。

s × 1/fS

以下よりも長い外部信号パルスは常に有効と判断され、フィルタ出力へ送られます。

(s + 1) × 1/fS

以下の範囲内の外部信号パルスは抑制される場合もあれば、有効と判断される場合もあります。

s × 1/fS～(s + 1) × 1/fS

DNFA<*name*>NFSTS[1:0]＝01B（同レベルのサンプル数：3）としたときのフィルタ動作例を次の図に示します。

<変更後>

DNFA<*name*>CTL.DNFA<*name*>NFSTS[1:0]で同レベルのサンプル数（2～5）を指定します。

s＝DNFA<*name*>NFSTS[1:0] + 2

以下よりも短い外部信号パルスは常に抑制されます。

(s – 1) × 1/fs

以下よりも長い外部信号パルスは常に有効と判断され、フィルタ出力へ送られます。

s × 1/fs

以下の範囲内の外部信号パルスは抑制される場合もあれば、有効と判断される場合もあります。

(s – 1) × 1/fs～s × 1/fs

DNFA<*name*>NFSTS[1:0]＝01B（同レベルのサンプル数：3）としたときのフィルタ動作例を次の図に示します。

(7)　RH850/ P1x-C

Section 2 Pin Functions

2.7.3.2 Digital filters

Digital filter characteristic

<Before>

DNFAnCTL.DNFAnNFSTS[1:0] determines the number s of same level samples (2 to 5):

External signal pulses, shorter than

DNFAnNFSTS[1:0] × 1/ fs

are always suppressed.

External signal pulses, longer than

(DNFAnNFSTS[1:0] + 1) × 1/ fs

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

DNFAnNFSTS[1:0] × 1/ fs to (DNFAnNFSTS[1:0] + 1) × 1/ fs

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e. s = 3 same level samples.

<After>

DNFAnCTL.DNFAnNFSTS[1:0] determines the number s of same level samples (2 to 5):

External signal pulses, shorter than

(DNFAnNFSTS[1:0] – 1) × 1/ fs

are always suppressed.

External signal pulses, longer than

DNFAnNFSTS[1:0] × 1/ fs

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

(DNFAnNFSTS[1:0] – 1) × 1/ fs to DNFAnNFSTS[1:0] × 1/ fs

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e. s = 3 same level samples.

(8)　RH850/ P1L-C

Section 2 Pin Functions

2.7.3.2 Digital filters

Digital filter characteristic

<Before>

DNFAnCTL.DNFAnNFSTS[1:0] determines the number s of same level samples (2 to 5):

External signal pulses, shorter than

DNFAnNFSTS[1:0] × 1/fs

are always suppressed.

External signal pulses, longer than

(DNFAnNFSTS[1:0] + 1) × 1/fs

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

DNFAnNFSTS[1:0] × 1/fs to (DNFAnNFSTS[1:0] + 1) × 1/fs

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e. s = 3 same level samples.

< After >

DNFAnCTL.DNFAnNFSTS[1:0] determines the number s of same level samples (2 to 5):

External signal pulses, shorter than

(DNFAnNFSTS[1:0] – 1) × 1/fs

are always suppressed.

External signal pulses, longer than

DNFAnNFSTS[1:0] × 1/fs

are always judged as valid and are passed on to the filter output.

Consequently, external signal pulses in the range

(DNFAnNFSTS[1:0] – 1) × 1/fs to DNFAnNFSTS[1:0] × 1/fs

may be suppressed or judged as valid.

The filter operation is illustrated in the figure below with DNFAnNFSTS[1:0] = 01B, i.e. s = 3 same level samples.

(9)　RH850/ U2Ax

Section 2　Pin Function

2.7.2.2 Digital Filters (1) Digital Filter Characteristic

<Before>

External signal pulses shorter than the following are always suppressed.

s × 1/fs

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

(s + 1) × 1/fs

External signal pulses in the following range may be suppressed or judged as valid.

s × 1/fs to (s + 1) × 1/fs

<After>

External signal pulses shorter than the following are always suppressed.

(s – 1) × 1/fs

External signal pulses longer than the following are always judged as valid and are passed on to the filter output.

s × 1/fs

External signal pulses in the following range may be suppressed or judged as valid.

(s – 1) × 1/fs to s × 1/fs

Section 55 Electrical Characteristics

55.3.6.2 Interrupt, Wake-up and Error Input Timing

Table 55.37 Interrupt Timing

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	*3	600			ns
		*4	20			μs
NMI input low level width	t_{WNIL}	*3	600			ns
		*4	20			μs
NMI pulse rejection width*2	t_{WNIRJ}		100		600	ns
INTPn input high level width	t_{WITH}	*3	600			ns
		*4	20			μs
INTPn input low level width	t_{WITL}	*3	600			ns
		*4	20			μs
INTPn pulse rejection width*2	t_{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t_{WRLINH}		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up input low level width	t_{WRLINL}		(S + 1) x 1/fs*1			ns
RLIN3nRX wake-up pulse rejection width*2	$t_{WRLINRJ}$		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
CANnRX wake-up input high level width	t_{WCANH}		(S + 1) x 1/fs*1			ns
CANnRX wake-up input low level width	t_{WCANL}		(S + 1) x 1/fs*1			ns
CANnRX wake-up pulse rejection width*2	t_{WCANRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
FLXnRXDA wake-up input high level width	t_{WFLXH}		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up input low level width	t_{WFLXL}		(S + 1) x 1/fs*1			ns
FLXnRXDA wake-up pulse rejection width*2	t_{WFLXRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
$\overline{\text{ERRORINn}}$ wake-up input high level width	t_{WERRH}		(S + 1) x 1/fs*1			ns
$\overline{\text{ERRORINn}}$ wake-up input low level width	t_{WERRL}		(S + 1) x 1/fs*1			ns
$\overline{\text{ERRORINn}}$ wake-up pulse rejection width*2	t_{WERRRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOSC/20)

Note 4. Level Detection (CLKA_LPS is operated by CLK_LSIOSC)

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high level width	t_{WNIH}	*3	600			ns
		*4	20			µs
NMI input low level width	t_{WNIL}	*3	600			ns
		*4	20			µs
NMI pulse rejection width*2	t_{WNIRJ}		100		600	ns
INTPn input high level width	t_{WITH}	*3	600			ns
		*4	20			µs
INTPn input low level width	t_{WITL}	*3	600			ns
		*4	20			µs
INTPn pulse rejection width*2	t_{WIRJ}		100		600	ns
RLIN3nRX wake-up input high level width	t_{WRLINH}		S x 1/fs *1			ns
RLIN3nRX wake-up input low level width	t_{WRLINL}		S x 1/fs *1			ns
RLIN3nRX wake-up pulse rejection width*2	$t_{WRLINRJ}$		(S – 1) x 1/fs*1		S x 1/fs *1	ns
CANnRX wake-up input high level width	t_{WCANH}		S x 1/fs *1			ns
CANnRX wake-up input low level width	t_{WCANL}		S x 1/fs *1			ns
CANnRX wake-up pulse rejection width*2	t_{WCANRJ}		(S – 1) x 1/fs*1		S x 1/fs *1	ns
FLXnRXDA wake-up input high level width	t_{WFLXH}		S x 1/fs *1			ns
FLXnRXDA wake-up input low level width	t_{WFLXL}		S x 1/fs *1			ns
FLXnRXDA wake-up pulse rejection width*2	t_{WFLXRJ}		(S – 1) x 1/fs*1		S x 1/fs *1	ns
$\overline{\text{ERRORINn}}$ wake-up input high level width	t_{WERRH}		S x 1/fs *1			ns
$\overline{\text{ERRORINn}}$ wake-up input low level width	t_{WERRL}		S x 1/fs *1			ns
$\overline{\text{ERRORINn}}$ wake-up pulse rejection width*2	t_{WERRRJ}		(S – 1) x 1/fs*1		S x 1/fs *1	ns

Note 1. S: Number of sampling times
fs: The value given by following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_LSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

Note 3. Edge Detection or Level Detection (CLKA_LPS is operated by CLK_HSIOSC/20)

Note 4. Level Detection (CLKA_LPS is operated by CLK_LSIOSC)

55.3.6.4 ADTRG Timing

Table 55.39 ADCJnTRGm Timing

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCJnTRGm input high level width	t_{WADH}		(S + 1) x 1/fs*1			ns
ADCJnTRGm input low level width	t_{WADL}		(S + 1) x 1/fs*1			ns
ADCJnTRGm pulse rejection width*2	t_{WADRJ}		(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_ADC, CLKA_ADC
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCJnTRGm input high level width	t_{WADH}		S x 1/fs *1			ns
ADCJnTRGm input low level width	t_{WADL}		S x 1/fs *1			ns
ADCJnTRGm pulse rejection width*2	t_{WADRJ}		(S – 1) x 1/fs*1		S x 1/fs *1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_ADC, CLKA_ADC
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

55.3.6.5 Communication Signal Timing

Table 55.40 Control Signal

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	$t_{WSENTIH}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
SENTnRX input low level width	$t_{WSENTIL}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
SENTnRX pulse rejection width	$t_{WSENTIRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns
PSI5nRX input high level width*2	$t_{WPSI5IH}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
PSI5nRX input low level width	$t_{WPSI5IL}$	Analog filter	600			ns
		Digital filter	(S + 1) x 1/fs*1			ns
PSI5nRX pulse rejection width*2	$t_{WPSI5IRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		(S + 1) x 1/fs*1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_HSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SENTnRX input high level width	$t_{WSENTIH}$	Analog filter	600			ns
		Digital filter	S x 1/fs *1			ns
SENTnRX input low level width	$t_{WSENTIL}$	Analog filter	600			ns
		Digital filter	S x 1/fs *1			ns
SENTnRX pulse rejection width	$t_{WSENTIRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		S x 1/fs *1	ns
PSI5nRX input high level width*2	$t_{WPSI5IH}$	Analog filter	600			ns
		Digital filter	S x 1/fs *1			ns
PSI5nRX input low level width	$t_{WPSI5IL}$	Analog filter	600			ns
		Digital filter	S x 1/fs *1			ns
PSI5nRX pulse rejection width*2	$t_{WPSI5IRJ}$	Analog filter	100		600	ns
		Digital filter	(S – 1) x 1/fs*1		S x 1/fs *1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLK_HSB
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered out or not). This characteristic is not tested in production.

55.3.22 Timer Timing

Table 55.75 Timer Input Timing

<Before>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t_{WTDIH}		(S + 1) x 1/fs *1			ns
TAUDnIm input low level width	t_{WTDIL}		(S + 1) x 1/fs *1			ns
TAUDnIm pulse rejection width*2	t_{WTDRJ}		(S – 1) x 1/fs *1		(S + 1) x 1/fs *1	ns
TAUJnIm input high level width	t_{WTJIH}	Analog noise filter	600*3			ns
		Digital noise filter	(S + 1) x 1/fs *1			ns
TAUJnIm input low level width	t_{WTJIL}	Analog noise filter	600*3			ns
		Digital noise filter	(S + 1) x 1/fs *1			ns
TAUJnIm pulse rejection width*2	t_{WTJRJ}	Analog noise filter	100		600*3	ns
		Digital noise filter	(S – 1) x 1/fs *1		(S + 1) x 1/fs *1	ns
TAPAnESO input high level width*4	t_{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs *1			ns
TAPAnESO input low level width*4	t_{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	(S + 1) x 1/fs *1			ns
TAPAnESO pulse rejection width*2, *4	t_{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	(S – 1) x 1/fs *1		(S + 1) x 1/fs *1	ns
ENCAnTINm input high level width	t_{WENIH}		(S + 1) x 1/fs *1			ns
ENCAnTINm input low level width	t_{WENIL}		(S + 1) x 1/fs *1			ns
ENCAnTINm pulse rejection width*2	t_{WENRJ}		(S – 1) x 1/fs *1		(S + 1) x 1/fs *1	ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI high level width	t_{WTGIH}		(S + 1) x 1/fs *1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI low level width	t_{WTGIL}		(S + 1) x 1/fs *1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI pulse rejection width*2	t_{WTGRJ}		(S – 1) x 1/fs *1		(S + 1) x 1/fs *1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLK_HSB (others)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not.
This characteristic is not tested in production.

Note 3. When CLK_LSIOSC is selected by CLKA_TAUJ register, at least one clock period of CLK_LSIOSC (4.6 µs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 µs width may be rejected.

Note 4. By-pass of filter is possible. For details, see **Section 2.7.2.10, ANF/DNF Type F1**.

<After>

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUDnIm input high level width	t_{WTDIH}		S x 1/fs *1			ns
TAUDnIm input low level width	t_{WTDIL}		S x 1/fs *1			ns
TAUDnIm pulse rejection width*2	t_{WTDRJ}		(S – 1) x 1/fs *1		S x 1/fs *1	ns
TAUJnIm input high level width	t_{WTJIH}	Analog noise filter	600*3			ns
		Digital noise filter	S x 1/fs *1			ns
TAUJnIm input low level width	t_{WTJIL}	Analog noise filter	600*3			ns
		Digital noise filter	S x 1/fs *1			ns
TAUJnIm pulse rejection width*2	t_{WTJRJ}	Analog noise filter	100		600*3	ns
		Digital noise filter	(S – 1) x 1/fs *1		S x 1/fs *1	ns
TAPAnESO input high level width*4	t_{WTPIH}	Analog noise filter	600			ns
		Digital noise filter	S x 1/fs *1			ns
TAPAnESO input low level width*4	t_{WTPIL}	Analog noise filter	600			ns
		Digital noise filter	S x 1/fs *1			ns
TAPAnESO pulse rejection width*2, *4	t_{WTPRJ}	Analog noise filter	100		600	ns
		Digital noise filter	(S – 1) x 1/fs *1		S x 1/fs *1	ns
ENCAnTINm input high level width	t_{WENIH}		S x 1/fs *1			ns
ENCAnTINm input low level width	t_{WENIL}		S x 1/fs *1			ns
ENCAnTINm pulse rejection width*2	t_{WENRJ}		(S – 1) x 1/fs *1		S x 1/fs *1	ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI high level width	t_{WTGIH}		S x 1/fs *1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI low level width	t_{WTGIL}		S x 1/fs *1			ns
TSG3nPTSIm/ENCAnEx, TSG3nCLKI pulse rejection width*2	t_{WTGRJ}		(S – 1) x 1/fs *1		S x 1/fs *1	ns

Note 1. S: Number of sampling times
fs: The value given by the following formula

$$fs = \frac{f_{DNFCK}}{PRS}$$

f_{DNFCK}: frequency of CLKA_TAUJ (for TAUJ2 and TAUJ3), CLK_HSB (others)
PRS: 1, 2, 4, 8, … , 128

Note 2. Input pulse shorter than the given min. value will be filtered out. Input pulses between min. and max. value result in an undefined signal condition (i.e. pulses might be filtered or not.
This characteristic is not tested in production.

Note 3. When CLK_LSIOSC is selected by CLKA_TAUJ register, at least one clock period of CLK_LSIOSC (4.6 µs) is required for activation of input signal for that domain. Any input pulses with less than 4.6 µs width may be rejected.

Note 4. By-pass of filter is possible. For details, see **Section 2.7.2.10, ANF/DNF Type F1**.

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4. 該非判定フロー

(1)	DNF を使用しているか？
(2)	抑制パルス幅と通過パルス幅の計算は式を使用しているか？