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RENESAS TECHNICAL UPDATE

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Title	Revised information of S3A7 User's Manual from Rev.1.00		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S3 Series S3A7	Lot No. All lots	Reference Document	S3A7 User's Manual: Microcontrollers, Rev.1.00		

1. Table 20.7 Register settings for input/output pin function (PORT2) (1)

• Modify NCODR bit and PCR bit of P200 to rewrite the register settings in the Table 20.7, step comparison as follows

[Before]

	Pin
	P200
ISEL bit	NMI
NCODR bit	✓
PCR bit	✓
DSCR bit	—

[After]

	Pin
	P200
ISEL bit	NMI
NCODR bit	—
PCR bit	—
DSCR bit	—

2. 11.9.6 Timing of WFI Instruction

[Before]

It is possible for the WFI instruction to be executed before I/O register writes are complete, in which case operation might not be as intended. This can happen if the WFI is placed immediately after a write to an I/O register. To avoid this problem, it is recommended that you read back the register that was written to confirm that the write has completed.

[After]

It is possible for the WFI instruction to be executed before I/O register and CS area writes are complete, in which case operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an I/O register and CS area. To avoid this problem, it is recommended that you read back the register and CS area that was written to confirm that the write completed.

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3. 22.2.1 POEG Group n Setting Register (POEGGn) (n = A to D)

• Modify the IOCE bit to rewrite bit name and description, step comparison as follows

[Before]

Bit	Symbol	Bit name	Description	R/W
b5	IOCE	Output-disable Request Enable from GPT or ACMPHS	0: Output-disable request from the GPT disable request or comparator interrupt disabled 1: Output-disable request from the GPT disable request or comparator interrupt enabled.	R/W*2

Note 2. Can be modified only once after a reset.

[After]

Bit	Symbol	Bit name	Description	R/W
b5	IOCE	Enable for GPT Output-disable Request	0: Disable output-disable requests from GPT disable request 1: Enable output-disable requests from GPT disable request.	R/W*2

Note 2. Can be modified only once after a reset.

4. 9.2.20 Clock Out Control Register (CKOCR)

[Before]

Set this bit to enable output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output. If the CKOSTP bit is rewritten while the clock is still oscillating, a glitch might be generated in the output.

[After]

Set this bit to enable output from the CLKOUT pin.

When this bit is set to 1, the selected clock is output. When this bit is set to 0, low is output.

When changing this bit, confirm that the clock source selected in the CKOSEL[3:0] bits is stable. Otherwise, a glitch might be generated in the output.

Note: This bit must be cleared before entering Software Standby mode if the selected clock source is stopped in that mode.

5. 9.2.12 Oscillation Stabilization Flag Register (OSCSF)

• Additional XXXXXX to rewrite the setting condition of HOCOSF flag in the section 9.2.12, step comparison as follows

[Before]

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

[Setting condition]

After the high-speed clock oscillator stops and the HOCOCR.HCSTP bit is set to 0, supply of the high-speed clock in the MCU starts after 287 cycles of the middle-speed clock are counted.

[After]

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

[Setting condition]

After the high-speed clock oscillator stops and the HOCOCR.HCSTP bit is set to 0, supply of the high-speed

clock in the MCU starts after the middle-speed clock cycles set in the HOCOWTCR.HSTS[2:0] bits elapse.

6. Additional Flash Patch and Break Unit

• Additional Flash Patch and Break Unit in the section 2.8, step comparison as follows

[Before]

No description.

[After]

2.8 Flash Patch and Break Unit

The MCU has a Flash Patch and Break unit. Breakpoint function is available but flash patch (remap) function is unavailable. Therefore, do not set the REPLACE bits (bits [31:30]) in the FP_COMPn register to 0. Bit [28] of the FP_REMAP register is fixed at 1. When writing to this register, write 1 to bit [28]. When reading this register, bit [28] is always read as 1. See reference 1. for details.

7. 51.9 POR and LVD Characteristics

• Modified LVD Hysteresis width (Electrical Characteristics).

[Before]

Table 51.63 Power-on reset circuit and voltage detection circuit characteristics (2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Hysteresis width (LVD1 and LVD2)	V_{LVH}	-	70	-	mV	V_{det1_0} to V_{det1_4} selected.
		-	60	-		V_{det1_5} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_D} selected.
		-	60	-		LVD2 selected.

[After]

Table 51.63 Power-on reset circuit and voltage detection circuit characteristics (2)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Hysteresis width (LVD0, LVD1 and LVD2)	V_{LVH}	-	60	-	mV	LVD0 selected
		-	100	-		V_{det1_0} to V_{det1_2} selected.
		-	60	-		V_{det1_3} to V_{det1_9} selected.
		-	50	-		V_{det1_A} to V_{det1_B} selected.
		-	40	-		V_{det1_C} to V_{det1_F} selected.
		-	60	-		LVD2 selected.

8. 23.9.2 Settings of GTCCRn during Compare Match Operation (n = A to F)

[Before]

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

• In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU

• In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVU

Similarly, the GTCCRE and GTCCRF registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

• In up-counting: GTCCRE < GTCCRF, GTCCRE > GTDVU, GTCCRF < GTPR - GTDVU

• In down-counting: GTCCRE > GTCCRF, GTCCRE < GTPR – GTDVU, GTCCRF > GTDVU

[After]

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

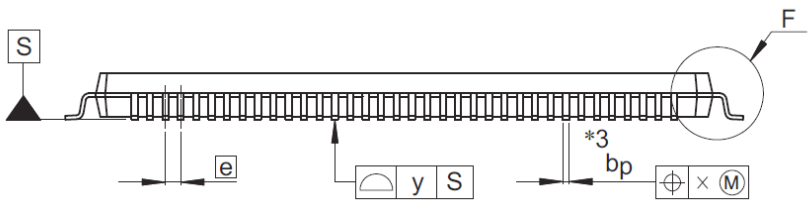
The GTCCRC and GTCCRD registers must be set to satisfy the following restrictions. If the restrictions are not satisfied, correct output waveforms with secured dead time may not be obtained.

• In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVU

• In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVU

9. Appendix 2. Package Dimensions

• Modified figure 2.2, LQFP 144-pin



[Before]

Reference symbol	Dimensions in millimeters		
	Min	Nom	Max
:	:	:	:
y	-	-	0.08
:	:	:	:

[After]

Reference symbol	Dimensions in millimeters		
	Min	Nom	Max
:	:	:	:
y	-	-	0.10
:	:	:	:

10. 20.2.1 Port Control Register 1

[Before]

20.2.1 Port Control Register 1 (PCNTR1)

PDR selects the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PDR bit. The I/O direction can be specified in 1-bit units.

[After]

20.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

Port Control Register 1 is 32- or 16-bit readable/writable register that controls the port direction and port output data. PCNTR1 specifies the port direction and the output data, which is accessed in 32-bit units. PODR (bits [31:16]) and PDR (bits [15:0]) are accessed in 16-bit units.

PDR selects the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PDR bit. The I/O direction can be specified in 1-bit units.

11. 20.2.2 Port Control Register 2

[Before]

20.2.2 Port Control Register 2 (PCNTR2)

PIDR reflects the individual pin states of the port, regardless of the values set in PORTm.PIDR and PORTm.PDR. When PORTm.PMR = 1 or PORTm.PDR = 1, the read data is don't care.

[After]

20.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

Port Control Register 2 allows read access to the port input data and the port event input data by 32- and 16-bit accesses. The PCNTR2 register specifies the port input data and the port event input data, which is accessed in 32-bit units. EIDR (bits 31 to 16 in PCNTR2) and PIDR (bits 15 to 0 in PCNTR2) respectively are accessed in 16-bit units.

PIDR reflects the individual pin states of the port, regardless of the values set in PORTm.PMR and PORTm.PDR. When PORTm.PMR = 1 or PORTm.PDR = 1, the read data is don't care.

12. 20.2.3 Port Control Register 3

[Before]

20.2.3 Port Control Register 3 (PCNTR3)

POSR changes PODR when set by a software write. For example, for P100, when PORT1.POSR00 = 1, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved.

[After]

20.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

(omitted)

Port Control Register 3 is a 32- and 16-bit writable register that controls the setting or resetting of the port output data. PCNTR3 controls the setting or resetting of the port output data, which is set by 32-bit units. PORR (bits 31 to 16 in PCNTR3) and POSR (bits 15 to 0 in PCNTR3) respectively, are accessed in 16-bit units.

POSR changes PODR when set by a software write. For example, for P100, when PORT1.POSR00 = 1, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved.

13. 20.2.4 Port Control Register 4

[Before]

20.2.4 Port Control Register 4 (PCNTR4)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.EOSR00 is set to 1 when ELC_PORTx occurs, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value must always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.b0, PORT2.PCNTR3.b14, and PORT2.PCNTR3.b15 are reserved.

[After]

20.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

Port Control Register 4 is a 32- or 16-bit readable/ writable register that controls the setting or resetting of the port output data by event input from the ELC. PCNTR4 is accessed in 32-units, while EORR (bits [31:16] in PCNTR4) and EOSR (bits [15:0] in PCNTR4) are accessed in 16-bit units.

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.EOSR00 is set to 1 when ELC_PORTx occurs, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value must always be 0. P200, P214, and P215 are input only, so PORT2.PCNTR3.b0, PORT2.PCNTR3.b14, and PORT2.PCNTR3.b15 are reserved.

14. 20.2.5 Port mn Pin Function Select Register (PmnPFS) (m = 0 to 9; n = 00 to 15)

[Before]

20.2.5 Port mn Pin Function Select Register (PmnPFS) (m = 0 to 9; n = 00 to 15)

(omitted)

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

[After]

20.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 9; n = 00 to 15)

(omitted)

Port mn Pin Function Select Register is a 32-, 16-, or 8-bit readable/writable control register that controls the selection of the port mn function. PmnPFS is set in 32-bit units, PmnPFS_HA (bits [15:0] in PmnPFS) is accessed in 16-bit units, and PmnPFS_BY (bits [7:0]) is accessed in 8-bit units.

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

15. 2.10.2.4 Connecting Sequence and JTAG/SWD Authentication

[Before]

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, OCD might be required to input the ID code to the authentication registers. The value of the OSIS in the Option Setting Memory decides whether the code is required or not.

(1) When OSIS is all 1s (Default)

OCD authentication is not required and OCD can use the AHB-AP without authentication.

(omitted)

(2) When OSIS is not all 1s

OCD authentication is required and OCD must write the unlock code to the IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

[After]

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, OCD might be required to input the ID code to the authentication registers. The value of the OSIS in the Option Setting Memory decides whether the code is required or not.

After negation of the reset, a wait period of 44 µs is needed before comparing the OSIS at cold start.

(1)When MSB of OSIS is 0 (Bit [127] = 0)

The ID code is always non-matching and connection to the on-chip debugger is prohibited.

(2) When OSIS is all 1s (Default)

OCD authentication is not required and OCD can use the AHB-AP without authentication.

(omitted)

(3) When OSIS is ALeRASE in ASCII code

The content of the user flash area is erased at once. See section 48, Flash Memory for details.

(4) When OSIS is not all 1s

OCD authentication is required and OCD must write the unlock code to the IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

16. 47.3.3 ECC Error Generation

[Before]

(omitted)

An ECC error can generate either a non-maskable interrupt or a reset, as selected in the ECCOAD register. When the OAD bit in the ECCOAD register is set to 1, an ECC error is output to the reset function. When the OAD bit in the ECCOAD register is set to 0, an ECC error is output to the ICU as a non-maskable interrupt. When the debugger is connected, reset and NMI interrupt do not occur. However, ECC 1-bit errors are corrected.

[After]

(omitted)

An ECC error can generate either a non-maskable interrupt or a reset, as selected in the ECCOAD register. When the OAD bit in the ECCOAD register is set to 1, an ECC error is output to the reset function. When the OAD bit in the ECCOAD register is set to 0, an ECC error is output to the ICU as a non-maskable interrupt.

17. 47.3.5 Parity Calculation Function

[Before]

Note: When a debugger is connected, reset and NMI interrupt do not occur.

[After]

<deleted>

18. 47.3.6 SRAM Error Sources

[Before]

Table 47.2 SRAM error sources

SRAM error source	DTC activation	DMAC activation
ECC error (SRAM0 area with ECC)	Not possible	Not possible
Parity error (SRAM0 area without ECC and SRAM1)	Not possible	Not possible

Reset and non-maskable interrupt do not occur when a debugger is connected. Other ECC functions are not affected by the debugger.

[After]

Table 47.2 SRAM error sources

SRAM error source	DTC activation	DMAC activation
ECC error (SRAM0 area with ECC)	Not possible	Not possible
Parity error (SRAM0 area without ECC and SRAM1)	Not possible	Not possible

19. 29.13.6 Restrictions on Clock-Synchronous Transmission (Clock-Synchronous Mode and Simple SPI Mode)

[Before]

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Update TDR by the CPU, DMAC, or DTC and wait for at least five PCLK cycles before allowing the transmit clock to be input (see Figure 29.77).

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock (bit 7) (see Figure 29.77).

When updating TDR after bit 7 starts to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit 7) to four PCLK cycles or longer (see Figure 29.77).

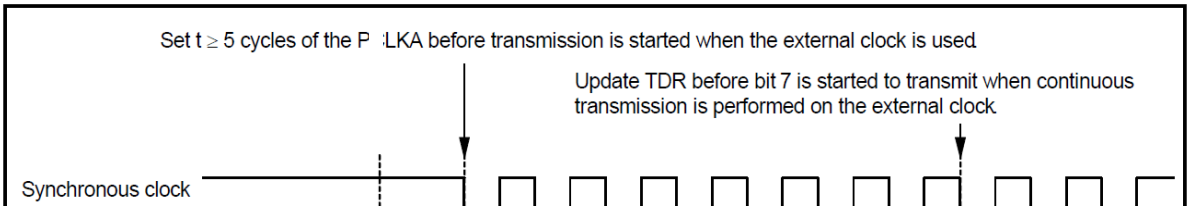


Figure 29.77 Restrictions on use of external clock in clock-synchronous transmission

[After]

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLK cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}). See figure 29.77.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock, bit [7], see Figure 29.77.

When updating TDR after bit [7] starts to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock, bit [7] to 4 PCLK cycles or longer, see Figure 29.77.

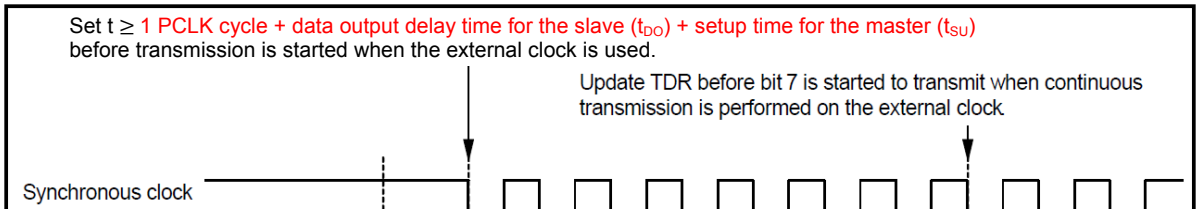


Figure 29.77 Restrictions on the use of external clock in clock synchronous transmission

20. 36.2.1 Control Register (SSICR)

[Before]

Bit	Symbol	Bit name	Description	R/W
:	:	:	:	:
b9	PDTA	Parallel Data Allocation *3	When data word length is 8 or 16 bits: 0: Lower bits of parallel data (SSIFTDR, SSIFRDR) transferred before upper bits 1: Upper bits of parallel data (SSIFTDR, SSIFRDR) transferred before lower bits. When data word length is 18, 20, 22, or 24 bits: 0: Parallel data (SSIFTDR, SSIFRDR) left-aligned 1: Parallel data (SSIFTDR, SSIFRDR) right-aligned.	R/W

[After]

Bit	Symbol	Bit name	Description	R/W
:	:	:	:	:
b9	PDTA	Parallel Data Allocation *3	When data word length is 8 or 16 bits: 0: Parallel data allocated at the lower bytes/half word (SSIFTDR, SSIFRDR) are transferred prior to the upper bytes/half word 1: Parallel data allocated at the upper bytes/half word (SSIFTDR, SSIFRDR) are transferred prior to the lower bytes/half word. When data word length is 18, 20, 22, or 24 bits: 0: Parallel data (SSIFTDR, SSIFRDR) left-aligned 1: Parallel data (SSIFTDR, SSIFRDR) right-aligned.	R/W

21. 11.8.4 Snooze Operation Example

[Before]

Table 11.9 and Table 11.10 are max transfer rate of SCI0 in Snooze mode.

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.9 HOCO: ± 1.0% (Ta = -20 to 85°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	9600	9600	-	
2			4800	2400
4				
8	4800	4800		
16				
32				
64				

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.10 HOCO: ± 1.5% (Ta = -40 to -20°C, 85 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency			
	24 MHz	32 MHz	48 MHz	64 MHz
1	2400		-	
2			2400	
4				
8				
16				
32				
64				

[After]

Table 11.9 and Table 11.10 are max transfer rate of SCI0 in Snooze mode. When SCI0 is used in the Snooze mode, the following settings must be used: BGDM = 0, ABCS = 0, ABCSE = 0. See section 29, Serial Communications Interface (SCI) for information on these bits.

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.9 HOCO: ± 1.0% (Ta = -20 to 85°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency			
	24MHz	32MHz	48MHz	64MHz
1	9600*1	-	-	-
2	9600*2	9600*4	4800	-
4	9600*3	9600*5	4800	2400
8	4800	4800	4800	2400
16	4800	4800	4800	2400
32	2400	2400	2400	2400
64	2400	2400	2400	2400

Note 1. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=3Dh, SCI0.MDDR = CEh must be used for 9600bps.
Note 2. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=1Eh, SCI0.MDDR = CEh must be used for 9600bps.
Note 3. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=0Dh, SCI0.MDDR = BAh must be used for 9600bps.
Note 4. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=32h, SCI0.MDDR = FEh must be used for 9600bps.
Note 5. SCI0.SMR.CKS[1:0]=00b, SCI0.SEMR.BRME=1, SCI0.BRR=18h, SCI0.MDDR = F9h must be used for 9600bps.

High-speed mode, Middle-speed mode, Low-speed mode

Table 11.10 HOCO: ± 2.0% (Ta = -40 to -20°C, 85 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency			
	24MHz	32MHz	48MHz	64MHz
1	2400	-	-	-
2	2400	2400	2400	-
4	2400	2400	2400	1200
8	2400	2400	2400	1200
16	2400	2400	2400	1200
32	1200	1200	1200	1200
64	1200	1200	1200	1200

22. 51.9 POR and LVD Characteristics

[Before]

t_{POR} specification is not defined.

[After]

Table 51.63 Power-on reset circuit and voltage detection circuit characteristics (2)

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after power-on reset cancellation	LVD0: enable	t_{POR}	-	1.7	-	ms	-
	LVD0: disable	t_{POR}	-	1.3	-	ms	

23. 29.2.23 I^2C Mode Register 3 (SIMR3)

[Before]

SIMR3.IICSTIF bit description

[Clearing conditions]

• Writing 0 to the bit (confirm that the IICSTIF flag is 1 before doing so).

• Writing 0 to the SIMR1.IICM bit (when operation is not in simple I^2C mode).

• Writing 0 to the SCR.TE bit.

[After]
SIMR3.IICSTIF bit description
[Clearing conditions]
• On writing 0 to the bit (after writing 0, confirm that the IICSTIF flag is 0)
• On writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode
• On writing 0 to the SCR.TE bit.

24. 29.5.6 Simultaneous Serial Data Transmission and Reception (Clock-Synchronous Mode)

[Before]
(2) FIFO selected
Figure 29.44 shows a sample flowchart for simultaneous serial transmit and receive operations in clock-synchronous mode at FIFO selected.
(omitted)
To switch from receive mode to simultaneous transmit and receive mode, check that the SCI completes the reception. Set the SCR.RIE and SCR.RE bits to 0. Check that the receive error flags ORER, FER, and PER in SSR_FIFO are 0, then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.

[After]
(2) FIFO selected
Figure 29.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.
(omitted)
To switch from receive mode to simultaneous transmit and receive mode:
1. Check that the SCI completes the reception.
2. Set the RIE and RE bits to 0.
3. Check that the receive error flag ORER in SSR_FIFO is 0, and then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.

25. 37.2.4 Data Stop Register (SD_STOP)

[Before]
STP bit (Transfer Stop)
(omitted)
• When STP is set to 1 after a command sequence is complete, CMD12 is not issued and the access end flag is not set.
• Set STP to 1 after the response end flag is set.
• Set STP to 0 after the response end flag is set.

[After]
STP bit (Transfer Stop)

(omitted)

- When STP is set to 1 after a command sequence is complete, CMD12 is not issued and the access end flag is not set.
- Set STP to 1 after the response end flag sets.
- Set STP to 0 after the access end flag sets.