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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RL*-A0127A/E	Rev.	1.00
Title	Restrictions on Usage of the DTC and RESF Register		Information Category	Technical Notification	
Applicable Product	RL78/G24 Group products	Lot No. All lots	Reference Document	RL78/G24 User's Manual: Hardware Rev.1.00 R01UH0961EJ0100 (Apr. 2023)	

This document is a notification of restrictions on the usage of the data transfer controller (DTC) and reset control flag register (RESF) in the applicable products.

1. Restriction on Usage of the Data Transfer Controller (DTC)

Transfer by the DTC does not proceed on detection of a voltage condition by the LVD when voltage detection by the voltage detector (LVD) is selected as a source for activating the DTC (by setting the DTCEN6.DTCENi2 bit to 1).

Table 27 - 4 Correspondences between Interrupt Sources and DTCENi[7:0] Bits

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	Reserved	INTP0	INTP1 Note 3	INTP2 Note 3	INTP3 Note 3	INTP4 Note 3	INTP5 Note 2	INTP6
DTCEN1	INTP7	Key input Note 4	A/D conversion end for input channel 0	UART0 reception transfer end/CSI01 transfer end or buffer empty/IIC01 transfer end Note 2	UART0 transmission transfer end/CSI00 transfer end or buffer empty/IIC00 transfer end Note 2	UART1 reception transfer end/CSI11 transfer end or buffer empty/IIC11 transfer end	UART1 transmission transfer end/CSI10 transfer end or buffer empty/IIC10 transfer end	UART2 reception transfer end/CSI21 transfer end or buffer empty/IIC21 transfer end
DTCEN2	UART2 transmission transfer end/CSI20 transfer end or buffer empty/IIC20 transfer end	DALI reception transfer end	DALI transmission transfer end	DALI bus power down detection	End of channel 0 timer array unit counting or capture	End of channel 1 timer array unit counting or capture	End of channel 2 timer array unit counting or capture	End of channel 3 timer array unit counting or capture
DTCEN3	RD2 timer compare match A0	RD2 timer compare match B0	RD2 timer compare match C0	RD2 timer compare match D0	RD2 timer compare match A1	RD2 timer compare match B1	RD2 timer compare match C1	RD2 timer compare match D1
DTCEN4	Valley detection in RD2 timer extended complementary PWM mode	Crest detection in RD2 timer extended complementary PWM mode	Completion of FAA operations	RG2 timer compare match A	RG2 timer compare match B	RG2 timer compare match C	RG2 timer compare match D	RJ0 timer underflow
DTCEN5	End of TMKB30 counting	End of TMKB31 counting	End of TMKB32 counting	FAA timing compare match 0	Fixed-cycle signal of realtime clock/alarm match detection	Interval signal detection of 32-bit interval timer	Comparator detection 0	Comparator detection 1
DTCEN6	Comparator detection 2	Comparator detection 3	A/D conversion end for input channel 1 Note 5	A/D conversion end for input channel 2 Note 5	A/D conversion end for input channel 3 Note 5	Voltage detection Note 1	Reserved	Reserved

Note 1. When bit 6 (LVD0SEL) of the user option byte (000C1H) is set to 0 or when bit 6 (LVD1SEL) of the voltage detection level register (LVIS) is set to 0

Workaround

Have the CPU accept the voltage detection interrupt and use CPU instructions to transfer the data when the voltage detection interrupt is to be used as a trigger for transfer of data by the DTC.

2. Restrictions on Usage of the Reset Control Flag Register (RESF)

The following two restrictions apply to reading of the RESF register.

Restriction 1:

The RESF register is not automatically cleared in response to reading the value of the RESF register. Any flags that were set at the point of reading will only be cleared once a reset due to another source or sources occurs. See the table below for details of the state of the RESF register.

State of the RESF Register

<table>
<tr><td rowspan="2"></td><td rowspan="2">State on RESET Input or Power-on Reset</td><td colspan="2">State on an Internal Reset</td><td rowspan="2">State after Reading of the RESF Register</td></tr>
<tr><td>When the RESF register is read before the internal reset</td><td>When the RESF register is not read before the internal reset</td></tr>
<tr><td>Restricted operation</td><td rowspan="2">Cleared to 0.</td><td>Any flags that were set and had remained set are automatically cleared and the flag corresponding to the source of the new internal reset is set.</td><td rowspan="2">The flag corresponding to the source of the internal reset is set while any other flags that had been set in response to other internal reset sources remain set.</td><td>The RESF register is not automatically cleared and any flags that were set will remain set.</td></tr>
<tr><td>Operation as stated in the User's Manual</td><td>The flag corresponding to the source of the internal reset is set.</td><td>Cleared to 0.</td></tr>
</table>

Restriction 2:

The IAWRF flag in the RESF register is set at the start of on-chip debugging.

Workarounds

Workaround for restriction 1:

Only treat the first value read from the RESF register after a reset as a valid value. Treat the second and subsequent values read from the RESF register before another reset as invalid.

Workaround for restriction 2:

Ignore the IAWRF flag in the RESF register at the start of on-chip debugging. Judge that a reset due to illicit memory access has occurred if all of the following conditions are satisfied during on-chip debugging.

1. The voltage on the V_{DD} pin is above V_{POR} at the time of a reset.
2. The signal on the RESET# pin is not at the low level at the time of a reset.
3. The only flag that is set in the RESF register after a reset is the IAWRF flag.

Note: Whether or not a reset is due to illicit memory access can be determined by simply checking the IAWRF flag in the RESF register when on-chip debugging is not in use.

Plan for Rectification

We are planning to modify the masks to lift these restrictions, and also change the part numbers for ordering to reflect this.

・Applicable products

All products of the RL78/G24 group (with ordering part numbers of R7F101Gxxxxxx#xx0; each x indicates a specific letter or numeral)

・Ordering part numbers

Before the change: R7F101Gxxxxxx#xx0

After the change: R7F101Gxxxxxx#xx1

Examples of ordering part numbers before and after the change

Part Numbers before the Change	Part Numbers after the Change
R7F101GLG2DFB#AA0	R7F101GLG2DFB#AA1
R7F101GLG3CFB#AA0	R7F101GLG3CFB#AA1

・Effects on packages, implementation, functions, quality, and reliability

Lifting of the restrictions will have no effects on packages, implementation of the product on a user's board, the flow of quality control, FIT, electrical characteristics, functions, quality, or reliability.

・How to identify the products

You can identify the products by the ordering part number printed on the packaging label. You can also send us the trace code printed on the device package so that we can refer to the production history data and provide you with the results. Contact your local Renesas sales representative for identification of the products by using the trace code.

・Estimated month of the change

Shipment of the modified products is scheduled to start from January 2024 or later.