RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU & MCU	Document No.	TN-V85-A031A/E	Rev.	1.00
Title	Restriction of Multiplex bus cycle.		Information Category	Technical Notification	
Applicable Product	V850E2/FL4 V850E2/FL4-H V850E2/FK4 V850E2/FK4-H	Lot No.	Reference Document	User's Manual and Data sheet of applicable product	
		ALL lots			

This document describes restriction items of user's manual and datasheet about external memory access timing (MEMC0CLK asynchronous/synchronous timing) as below.

■ Restriction

(1) Added prohibited item at the MEMC0CLK synchronous

The setting of WAIT=0 is prohibited at the external memory access of MEMC0CLK synchronous.

According to this change, data input setup time (from MEMC0CLK (r)) is changed for "10+1T" at the external memory access of MEMC0CLK synchronous. Please refer to table-1, 2.

(2) Changed MEMC0WAIT hold time at the MEMC0CLK asynchronous

Minimum value of MEMC0WAIT hold time of external memory access "tHSTWT1" and "tHSTWT2" are changed.

Please refer to the table-3.

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■ Modifications of manual

Restriction (1)

On the User's Manual Chapter 4.3.4 [DWC0, DWC1 registers content], "No data wait" is prohibited as below.

Before correction

DWn3	DWn2	DWn1	DWn0	Number of data wait states
0	0	0	0	No data wait

After correction

DWn3	DWn2	DWn1	DWn0	Number of data wait states
0	0	0	0	Prohibited

Table-1 DWC0, DWC1 registers content

MEMC0CLK synchronous timing of datasheet is changed as below.

Before correction

Parameter	Symbol		Condition	MIN.	TYP.	MAX.	Unit
Data input setup time (from MEMC0CLK (r))	t_{SIDK}	⟨22⟩		10			ns

After correction

Parameter	Symbol		Condition	MIN.	TYP.	MAX.	Unit
Data input setup time (from MEMC0CLK (r))	t_{SIDK}	⟨22⟩		10 **+ 1T**			ns

Table-2 MEMC0CLK synchronous timing

(2) About limitation item of 2.

MEMC0CLK asynchronous timing of datasheet is changed as below.

Before correction

Parameter	Symbol		Condition	MIN.	TYP.	MAX.	Unit
MEMC0WAITZ hold time from MEMC0ASTBZ (f)	t_{HSTWT1}	⟨16⟩	w ≧ 1	$(w + AHW)T - (2HEAPCLK + 20)$			ns
	t_{HSTWT2}	⟨17⟩	w ≧ 1	$(1 + w + AHW)T - (2HEAPCLK + 20)$			ns

After correction

Parameter	Symbol		Condition	MIN.	TYP.	MAX.	Unit
MEMC0WAITZ hold time from MEMC0ASTBZ (f)	t_{HSTWT1}	⟨16⟩	w ≧ 1	$(w + AHW)T - (2HEAPCLK + $ **7.5**$)$			ns
	t_{HSTWT2}	⟨17⟩	w ≧ 1	$(1 + w + AHW)T - (2HEAPCLK + $ **7.5**$)$			ns

Table-3 MEMC0CLK asynchronous timing