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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0137A/E	Rev.	1.00
Title	RA8D1 Group, correction of correction of the description of the table and registers when FSBL is executed		Information Category	Technical Notification		
Applicable Product	RA8D1 Group	Lot No. All	Reference Document	RA8D1 Group User's Manual : Hardware Rev.1.20		

The description of table and registers are corrected when FSBL is executed as follows.:

Contents

1. 2.6 Initial Vector Table Base Address

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Table2.5 is corrected. The secure vector table base address is 0x0200_0000 regardless of FSBL execution.

Before correction

Table 2.5 Initial vector table base address

Operating mode	CPU INITSVTOR
Single-chip mode (not execute FSBL)	0x0200_0000
Single-chip mode (execute FSBL)	0x0700_0000

After correction

Table 2.5 Initial vector table base address

Operating mode	CPU INITSVTOR
Single-chip mode	0x0200_0000

2. 6.2.5 OFS1, OFS1_SEC: Option Function Select Register 1 for Non-secure and Secure

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The function of OFS1. HOCOEN is corrected.

Before correction

Address: OFS1: 0x1300_A180 (Non-secure)
OFS1_SEC: 0x0300_A200 (Secure)

Bit	Symbol	Function	R/W
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset	R

After correction

Address: OFS1: 0x1300_A180 (Non-secure)

Bit	Symbol	Function	R/W
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset When FSBL is executed, OFS1.HOCOEN register value needs to be “1”.	R

Address: OFS1_SEC: 0x0300_A200 (Secure)

Bit	Symbol	Function	R/W
8	HOCOEN	HOCO Oscillation Enable 0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset	R

3. 6.2.6 OFS1_SEL: Option Function Select Register 1 for Security Attribution

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The function of OFS1_SEL. HOCOEN and OFS1_SEL. HOCOFRQ0[2:0] are corrected.

Before correction

Bit	Symbol	Function	R/W
8	HOCOEN	Security attributes of HOCO Oscillation Enable 0: Select OFS1_SEC.HOCOEN 1: Select OFS1.HOCOEN	R
11:9	HOCOFRQ0[2:0]	Security attributes of HOCO Frequency Setting 0 0 0 0: Select OFS1_SEC.HOCOFRQ0[2:0] 1 1 1: Select OFS1.HOCOFRQ0[2:0] Others: Reserved	R

After correction

Bit	Symbol	Function	R/W
8	HOCOEN	Security attributes of HOCO Oscillation Enable 0: Select OFS1_SEC.HOCOEN 1: Select OFS1.HOCOEN Note: If FSBL is executed in reset, OFS1.HOCOEN is always selected regardless of this bit value.	R
11:9	HOCOFRQ0[2:0]	Security attributes of HOCO Frequency Setting 0 0 0 0: Select OFS1_SEC.HOCOFRQ0[2:0] 1 1 1: Select OFS1.HOCOFRQ0[2:0] Others: Reserved Note: If FSBL is executed in reset, OFS1.HOCOFRQ0 is always selected regardless of this bit-field value.	R

4. 6.2.16 SAMR : Start Address of Measurement Report

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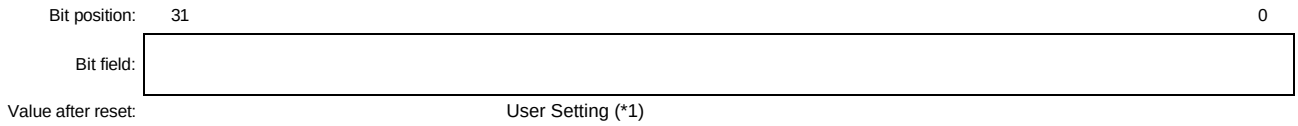
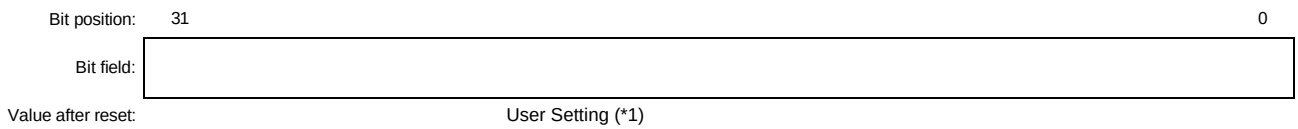
The setting address area of SAMR is corrected. This register is only used when FSBL is executed.

Before correction



Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

After correction



Note 1. The value in a blank product is 0xFFFFFFFF. It is set to the value written by your application.

The SAMR register specifies the starting address of measurement report. The measurement report is stored in the SRAM shown in Figure 43.14 Format and location of the measurement report. Specify Either SRAM0 or SRAM1 or Standby RAM. In case SRAM0 is used for measurement report, do not specify the addresses from 0x22007780 to 0x22007BFF. When reading the measurement report in SRAM0, disable the ECC functionality by setting SRAMCR0.ECCMOD[1:0]=b00.

5. 10.2.7 Module Stop Control Register C (MSTPCRC)

MSTCRC the value after reset in case FBSL is executed is corrected.

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Before correction

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	—	MSTPC27	MSTPC26	—	—	—	—	—	—	—	—	—	MSTPC16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	MSTPC12	MSTPC11	MSTPC10	—	MSTPC8	MSTPC7	MSTPC6	—	MSTPC4	—	—	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

After correction

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:	MSTPC31	—	—	—	MSTPC27	MSTPC26	—	—	—	—	—	—	—	—	—	MSTPC16
Value after reset:	1/0(*1)	1	1	1	1/0(*1)	1/0(*1)	1	1	1	1	1	1	1	1	1	1/0(*1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	MSTPC14	MSTPC13	MSTPC12	MSTPC11	MSTPC10	—	MSTPC8	MSTPC7	MSTPC6	—	MSTPC4	—	—	MSTPC1	MSTPC0
Value after reset:	1	1/0(*1)	1/0(*1)	1/0(*1)	1/0(*1)	1/0(*2)	1	1/0(*1)	1/0(*1)	1/0(*1)	1	1/0(*1)	1	1	1/0(*1)	1/0(*1)

Note*1): If FSBL is skipped in reset, then value after reset is 1, if FSBL is executed in reset, then value after reset is 0.

Note *2): If FSBL is skipped in reset, then MSTPC10 value after reset is 1. If FSB is executed in reset, then the value after reset depends on the parts number which supports MIPI DSI or not. If FSBL is executed in reset, then value after reset is 0 for R7FA8D1BHECBD, R7FA8D1BHECFC, R7FA8D1BFECBD, R7FA8D1BFECFC, which supports MIPI DSI, value after reset is 1 for R7FA8D1AHECBD, R7FA8D1AHECFC, R7FA8D1AFECBD, R7FA8D1AFECFC which does not support MIPI DSI.

Other update from this correction in Hardware Use's Manual

In CAC, CRC, GLCDC, DRW, SSIE1, SSIE0, MIPI DSI, SDHI/MMC1, SDHI/MMC0, DOC, ELC, CEU, CANFD1, CANFD0, RSIP-E51A explanation chapter, there is a note that each module is stopped after reset. This is also corrected as the initial Module-stop state is defined by MSTPCRC.

6. 41.2.4 CRC Data Output Register(CRCDOR/CRCDOR_HA/CRCDOR_BY)

[Page 2221]

Before correction

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Function	R/W
31:0	n/a	CRC output data The CRCDOR register is a 32-bit read/write register for CRC-32 or CRC-32C calculation. The CRCDOR_HA (CRCDOR[31:16]) register is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. The CRCDOR_BY (CRCDOR[31:24]) register is an 8-bit read/write register for CRC-8 calculation. Because its initial value is 0x00000000, rewrite the CRCDOR/CRCDOR_HA/ CRCDOR_BY register to perform the calculations using a value other than the initial value. Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0x00000000, there is no CRC error.	R/W

After correction

Bit position:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Bit field:																
Value after reset:	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:																
Value after reset:	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)	0/1(*1)

Note *1): If FSBL is executed in reset, then value after reset is 1, if FSBL is skipped in reset, then values after reset is 0.

Bit	Symbol	Function	R/W
31:0	n/a	CRC output data The CRCDOR register is a 32-bit read/write register for CRC-32 or CRC-32C calculation. The CRCDOR_HA (CRCDOR[31:16]) register is a 16-bit read/write register for CRC-16 or CRC-CCITT calculation. The CRCDOR_BY (CRCDOR[31:24]) register is an 8-bit read/write register for CRC-8 calculation. Rewrite the CRCDOR/CRCDOR_HA/ CRCDOR_BY register to perform the calculations using a value other than the initial value. Data written to the CRCDIR/CRCDIR_BY register is CRC calculated and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following the transferred data and the result is 0x00000000, there is no CRC error.	R/W

7. Setting if FSBL is executed in reset

If FSBL execution is selected in reset, this setting is required.

1. OFS1.HOCOEN needs to be used as oscillation disabled after reset. Therefore, OFS1.HOCOEN register value needs to be “1”.

8. Workarounds if FSBL is executed in reset

If FSBL execution is selected in reset, these are workarounds. If FSBL skipped in reset, no workaround is required.

1. The secure vector table base address is 0x0200_0000.

2. OFS1_SEL.HOCOEN and OFS1_SEL.HOCOFRQ0 always select OFS1.HOCOEN and OFS1.HOCOFRQ0 respectively. Therefore, Use HOCOCR and HOCOCR2, or OFS1.HOCOFREQ0 register to operate, stop and set frequency for HOCO.

3. In case SRAM0 is used for measurement report, do not specify the addresses from 0x22007780 to 0x22007BFF. When reading the measurement report in SRAM0, disable the ECC functionality by setting SRAMCR0.ECCMOD[1:0]=b00.

4. MSTPC0, MSTPC1, MSTPC4, MSTPC6, MSTPC7, MSTPC8, MSTPC11, MSTPC12, MSTPC13, MSTPC14, MSTPC16, MSTPC26, MSTPC27, MSTPC31 value after reset is 0. The corresponding module is not stopped. MSTPC10 may be 0 depending on the parts number. If the corresponding module is not in use, change respective module stop bit to 1 in order to reduce current consumption.

5. CRCDOR register’s initial value is not 0x00000000. Rewrite the CRCDOR/CRCDOR_HA/ CRCDOR_BY register to perform the CRC calculations using a value other than the value after reset.