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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0132A/E	Rev.	1.00
Title	RA0E1 Description in the User's Manual: Hardware Rev.1.00 Changed.		Information Category	Technical Notification		
Applicable Product	RA0E1 Group	Lot No. All	Reference Document	RA0E1 Group User's Manual: Hardware Rev.1.00 (R01UH1040EJ0100)		

This document describes misstatements found in the RA0E1 User's Manual: Hardware Rev. 1.00 (R01UH1040EJ0100).

Corrections

Applicable Item	Applicable Page	Contents	Pages in this document for corrections
Table 5.5 States of LOCO when a reset occurs	Page 60	Incorrect descriptions revised	Page 2
Figure 9.1 Low power mode transitions	Page 105	Incorrect descriptions revised	Page 3
Table 11.1 ICU specifications	Page 124	Incorrect descriptions revised	Page 4, Page 5
13.2 Usage Notes	Page 152	Incorrect descriptions revised	Page 6
17.1 Overview	Page 207	Incorrect descriptions revised	Page 7, Page 8
21.3.22 SO1: Serial Output Register 1	Page 361	Incorrect descriptions revised	Page 9, Page 10
25.2.3 ADM2: A/D Converter Mode Register 2	Page 574	Incorrect descriptions revised	Page 11
25.2.6 ADS: Analog Input Channel Specification Register	Page 578	Incorrect descriptions revised	Page 12
Figure 25.13 Example of software trigger wait mode (select mode, one-shot conversion mode) operation timing	Page 587	Incorrect descriptions revised	Page 13
25.7 Snooze Mode Function	Page 605	Incorrect descriptions revised	Page 14
25.7.1 A/D Conversion by Inputting a Software Trigger	Page 605 Page 606	Incorrect descriptions revised	Page 15 Page 16
Figure 25.25 Block diagram when using Snooze mode in hardware trigger wait mode	Page 607	Incorrect descriptions revised	Page 17
Table 28.5 Mapping for the extra bit of the startup area selection and security setting (address (P/E) :0x0000_0010)	Page 633	Incorrect descriptions revised	Page 18
Table 28.6 Mapping for the extra bit of the access window information program (address (P/E) :0x0000_0010)	Page 633	Incorrect descriptions revised	Page 19
28.3.25 PNRn : Part Numbering Register n (n = 0 to 3)	Page 641	Incorrect descriptions revised	Page 20, Page 21
Table 28.15 Basic functions	Page 644	Incorrect descriptions revised	Page 22
29 True Random Number Generator (TRNG)	Page 666	Incorrect descriptions revised	Page 23
Table 31.1 Absolute maximum ratings	Page 668	Incorrect descriptions revised	Page 24, Page 25
Table 31.11 I/O other characteristics	Page 674 Page 675	Incorrect descriptions revised	Page 26, Page 27
Table 31.12 Operating and standby current (1) (2 of 2)	Page 677	Incorrect descriptions revised	Page 28 Page 29
Table 31.16 Reset timing (2 of 2)	Page 684	Incorrect descriptions revised	Page 30
Figure 31.11 Reset input timing (2)	Page 684	Incorrect descriptions revised	Page 31
Table 31.46 LVD1 characteristics (2 of 2)	Page 719	Incorrect descriptions revised	Page 32

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

[Before correction of Table 5.5 States of LOCO when a reset occurs] (Page 60)

Table 5.5 States of LOCO when a reset occurs

		Reset source	
		POR/LVD0/LVD1	Other
LOCO	Enable or disable	Initialized to enable	

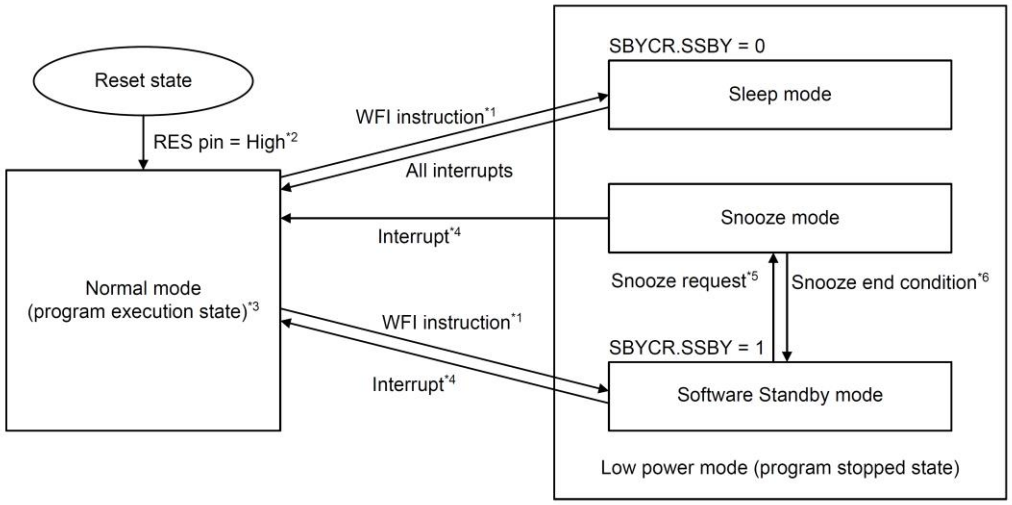
[After correction of Table 5.5 States of LOCO when a reset occurs]

Table 5.5 States of LOCO when a reset occurs

		Reset source	
		POR/LVD0/LVD1	Other
LOCO	Enable or disable	Initialized to disable. However, during IWDT operation, LOCO oscillates regardless of the value of LCSTP.	

[Before correction of Figure 9.1 Low power mode transitions] (Page 105)

Figure 9.1 shows the transition between Normal mode to low power mode.

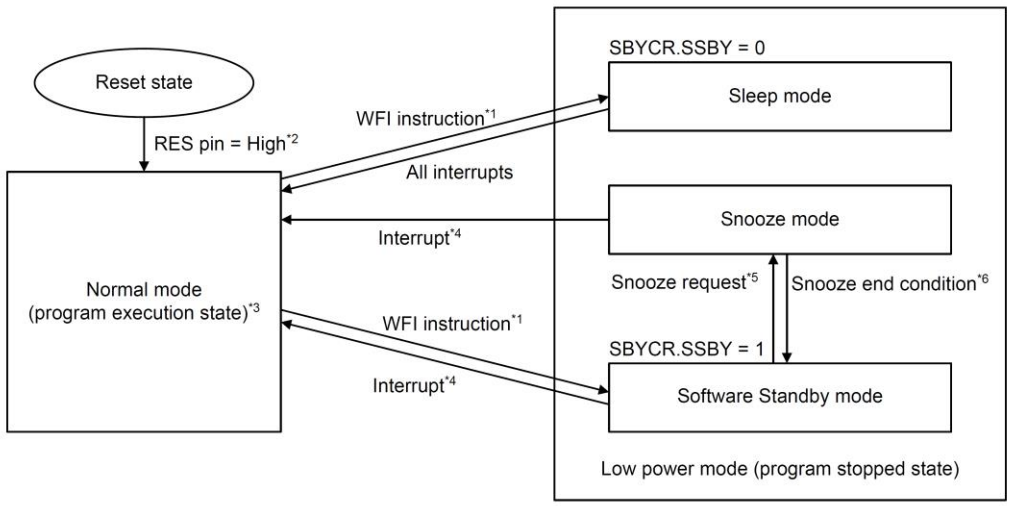


Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of a transition to low power mode.
Note 2. The MOCO is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made from an interrupt in Sleep mode, Software Standby mode, or Snooze mode. The clock source is the same as before entering the low power mode.
Note 4. See Table 9.3.
Note 5. See section 9.8.1. Transition to Snooze Mode.
Note 6. See section 9.8.3. Returning from Snooze Mode to Software Standby Mode.

Figure 9.1 Low power mode transitions

[After correction of Figure 9.1 Low power mode transitions]

Figure 9.1 shows the transition between Normal mode to low power mode.



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of a transition to low power mode.
Note 2. The HOCO is the source of the operating clock following a transition from the reset state to Normal mode.
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Note 6. See section 9.8.3. Returning from Snooze Mode to Software Standby Mode.

Figure 9.1 Low power mode transitions

[Before correction of Table 11.1 ICU specifications] (Page 124)

11. Interrupt Controller Unit (ICU)

11.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

Table 11.1 lists the ICU specifications, Figure 11.1 shows a block diagram, and Table 11.2 lists the I/O pins.

Table 11.1 ICU specifications

Item		Description
Maskable interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 33
	External pin interrupts	• Interrupt detection on falling edge, rising edge, rising and falling edges. One of these detection methods can be set for each source • 6 sources, with interrupts from IRQi (i = 0 to 5) pins.
	Interrupt requests to CPU (NVIC)	• 39 interrupt requests are output to NVIC.
	DTC control	• The DTC can be activated using interrupt sources*1 • The method for selecting an interrupt source is the same as that of the interrupt request to NVIC.
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Low voltage detection 1*3	Voltage monitor 1 interrupt of the voltage monitor 1 circuit (LVD_LVD1)
	RPEST	Interrupt on SRAM parity error
Low power modes		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SBYEDCRn register. • Snooze mode: return is initiated by non-maskable interrupts. Interrupt can be selected in the SBYEDCRn register. See section 11.2.14. SBYEDCR0 : Software Standby/Snooze End Control Register 0 and section 11.2.15. SBYEDCR1 : Software Standby/Snooze End Control Register 1.

Note 1. For the DTC activation sources, see Table 11.5.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as maskable interrupts. When used as maskable interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 interrupts, set the LVD1CR1.IRQSEL bits to 1.

[After correction of Table 11.1 ICU specifications]

11. Interrupt Controller Unit (ICU)

11.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the Nested Vector Interrupt Controller (NVIC), and the Data Transfer Controller (DTC) modules. The ICU also controls non-maskable interrupts.

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	Interrupt requests to CPU (NVIC)	• 39 interrupt requests are output to NVIC.
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Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge
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Low power modes		• Sleep mode: return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: return is initiated by non-maskable interrupts or any other interrupt source. Interrupt can be selected in the SBYEDCRn register. • Snooze mode: return is initiated by non-maskable interrupts or any other interrupt source. Interrupt can be selected in the SBYEDCRn register. See section 11.2.14. SBYEDCR0 : Software Standby/Snooze End Control Register 0 and section 11.2.15. SBYEDCR1 : Software Standby/Snooze End Control Register 1.

Note 1. For the DTC activation sources, see Table 11.5.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as maskable interrupts. When used as maskable interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 interrupts, set the LVD1CR1.IRQSEL bits to 1.

[Before correction of 13.2 Usage Notes] (Page 152)

13.2 Usage Notes

13.2.1 Notes on the Use of a Debugger

The memory cannot be debugged if the FRP is enabled. Disable the flash read protection when debug a program, OCD debug only valid when OFS1.FRPDIS bit is 1.

13.2.2 Compiler Settings

The FRP is a kind of execute-only memory (XOM). Since data in a protected region is not readable, a protected region cannot have constant data such as literal pool. Therefore, appropriate compiler settings are required.

[After correction of 13.2 Usage Notes]

13.2 Usage Notes

13.2.1 Notes on the Use of a Debugger

The memory cannot be debugged if the FRP is enabled. Disable the flash read protection when debug a program, OCD debug only valid when OFS1.FRPDIS bit is 1.

13.2.2 Compiler Settings

The FRP is a kind of execute-only memory (XOM). Since data in a protected region is not readable, a protected region cannot have constant data such as literal pool. Therefore, appropriate compiler settings are required.

13.2.3 Protection of OFS1 Register

Because overwriting OFS1.FRPS[5:0], OFS1.FRPE[5:0], or OFS1.FRPDIS bits can disable the protection of the FRP, OFS1 register (address = 0x0000_0404) must be protected by the access window function. However, setting the access window function, which includes setting AWS.FSPR bit to 0, also disables changing AWS.BTFLG and FISR.SAS[1:0] bits used for the startup area select function. Therefore, the startup area select function is not available when using the FRP function. See section 28.5.2. Startup Area Select for the startup area select function and section 28.5.3. Protection by Access Window for

[Before correction of 17.1 Overview] (Page 207)

17. Timer Array Unit (TAU)

17.1 Overview

The timer array unit has eight 16-bit timers.

Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be used to create a high-resolution timer.

Figure 17.1 shows the channel configuration per unit in timer array unit.

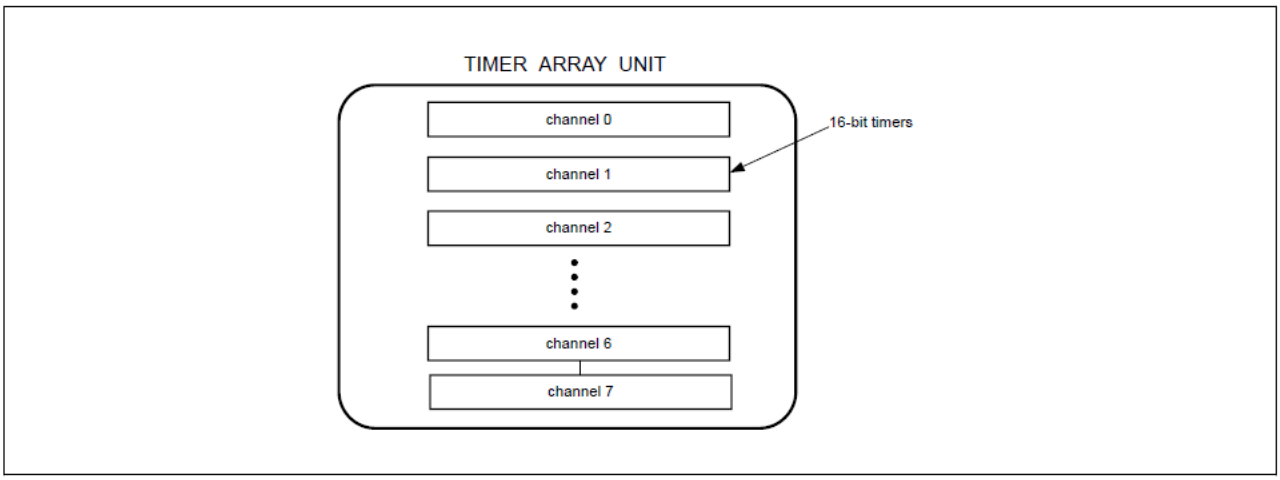

Figure 17.1 Channel configuration per unit

It is possible to use the 16-bit timer of channels 1 and 3 of unit 0 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer (upper or lower 8-bit timer) and square wave output (lower 8-bit timer only)
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 7 of unit 0 can be used to realize LIN-bus communication operating in combination with UART2 of the serial array unit.

The peripheral module clock (PCLKB) is equal to the system clock (ICLK) in RA0E1.

Table 17.1 lists the TAU functions and Figure 17.2 to Figure 17.11 show each functional image.

[After correction of 17.1 Overview]

17. Timer Array Unit (TAU)

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Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be used to create a high-resolution timer.

Figure 17.1 shows the channel configuration per unit in timer array unit.

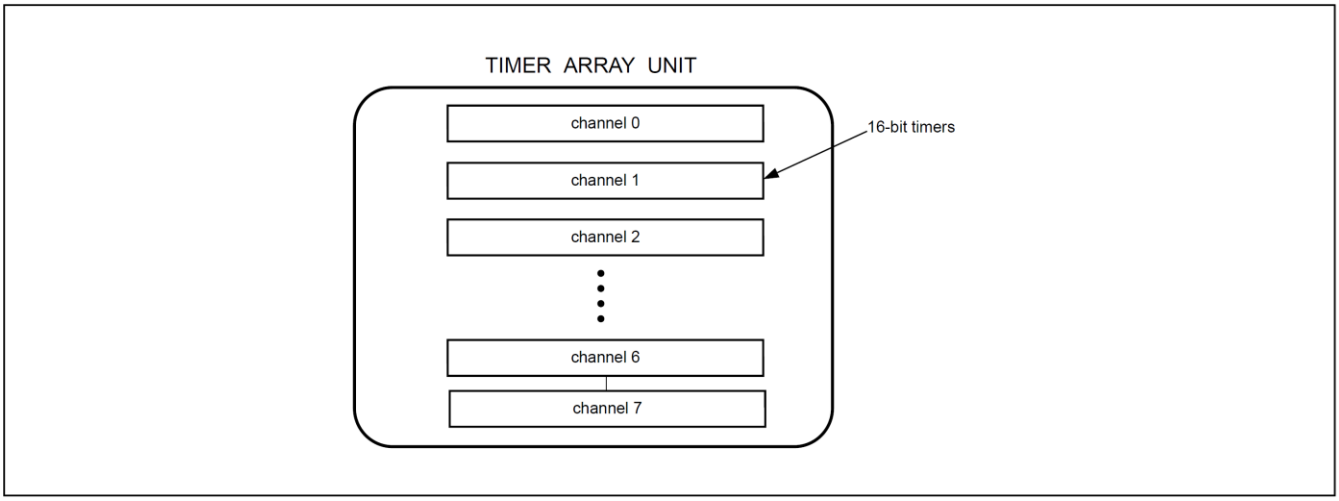


Figure 17.1 Channel configuration per unit

It is possible to use the 16-bit timer of channels 1 and 3 of unit 0 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer (upper and lower 8-bit timer) and square wave output (lower 8-bit timer only)
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 7 of unit 0 can be used to realize LIN-bus communication operating in combination with UART2 of the serial array unit.

The peripheral module clock (PCLKB) is equal to the system clock (ICLK) in RA0E1.

Table 17.1 lists the TAU functions and Figure 17.2 to Figure 17.11 show each functional image.

[Before correction of 21.3.22 SO1: Serial Output Register 1] (Page 361)

21.3.22 SO1: Serial Output Register 1

Base address: SAU1 = 0x400A_2200

Offset address: 0x0128

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CKO[1:0]		—	—	—	—	—	—	SO[1:0]	
Value after reset:	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1

Bit	Symbol	Function	R/W
1:0	SO[1:0]	Serial Data Output of Channel n 0: Serial data output value is 0 1: Serial data output value is 1	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CKO[1:0]	Serial Clock Output of Channel n 0: Serial clock output value is 0 1: Serial clock output value is 1	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

The SO1 is a buffer register for serial output of each channel of serial array unit 1.

The value of the SO[n] bit of this register is output from the serial data output pin of channel n.

The value of the CKO[n] bit of this register is output from the serial clock output pin of channel n.

The SO[n] bit of this register can be rewritten by software only when serial output is disabled (SOE1.SOE[n] = 0). When serial output is enabled (SOE1.SOE[n] = 1), rewriting by software is ignored, and the value of the register can be changed only by a serial communication operation.

The CKO[n] bit of this register can be rewritten by software only when the channel operation is stopped (SE1.SE[n] = 0). While channel operation is enabled (SE1.SE[n] = 1), rewriting by software is ignored, and the value of the CKO[n] bit can be changed only by a serial communication operation.

To use the pin for serial interface as a port function pin, set the corresponding CKO[n] and SO[n] bits to 1.

[After correction of 21.3.22 SO1: Serial Output Register 1]

21.3.22 SO1: Serial Output Register 1

Base address: SAU1 = 0x400A_2200

Offset address: 0x0128

Bit position:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit field:	—	—	—	—	—	—	CKO[1:0]		—	—	—	—	—	—	SO[1:0]	
Value after reset:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1

Bit	Symbol	Function	R/W
1:0	SO[1:0]	Serial Data Output of Channel n 0: Serial data output value is 0 1: Serial data output value is 1	R/W
7:2	—	These bits are read as 0. The write value should be 0.	R/W
9:8	CKO[1:0]	Serial Clock Output of Channel n 0: Serial clock output value is 0 1: Serial clock output value is 1	R/W
15:10	—	These bits are read as 0. The write value should be 0.	R/W

The SO1 is a buffer register for serial output of each channel of serial array unit 1.

The value of the SO[n] bit of this register is output from the serial data output pin of channel n.

The value of the CKO[n] bit of this register is output from the serial clock output pin of channel n.

The SO[n] bit of this register can be rewritten by software only when serial output is disabled (SOE1.SOE[n] = 0). When serial output is enabled (SOE1.SOE[n] = 1), rewriting by software is ignored, and the value of the register can be changed only by a serial communication operation.

The CKO[n] bit of this register can be rewritten by software only when the channel operation is stopped (SE1.SE[n] = 0). While channel operation is enabled (SE1.SE[n] = 1), rewriting by software is ignored, and the value of the CKO[n] bit can be changed only by a serial communication operation.

To use the pin for serial interface as a port function pin, set the corresponding CKO[n] and SO[n] bits to 1.

[Before correction of 25.2.3 ADM2: A/D Converter Mode Register 2] (Page 574)

AWC bit (Specification of the Snooze Mode)

This bit is used for specification of the Snooze mode.

When there is a hardware trigger signal in the Software Standby mode, the Software Standby mode is exited, and A/D conversion is performed without operating the CPU (the Snooze mode).

- When using the Snooze mode function, set AWC to 0 in software trigger wait mode, and set AWC to 1 in hardware trigger wait mode.
- Using the Snooze mode function in the software trigger no-wait mode or hardware trigger no-wait mode is prohibited.
- Using the Snooze mode function in the software trigger no-wait mode, software trigger wait mode, or hardware trigger no-wait mode is prohibited..
- When using the Snooze mode function, specify a hardware trigger interval of at least "shift time to Snooze mode*1 + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 PCLKB clock cycles + 5 µs".
- Even when using Snooze mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to Software Standby mode.
  Also, be sure to change the AWC bit to 0 after returning from Software Standby mode to normal operation.
  If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent Snooze mode or normal operation.

Note 1. Refer to Table 31.21 in section 31.4.2. Wakeup Time.

[After correction of 25.2.3 ADM2: A/D Converter Mode Register 2]

AWC bit (Specification of the Snooze Mode)

This bit is used for specification of the Snooze mode.

When there is a hardware trigger signal in the Software Standby mode, the Software Standby mode is exited, and A/D conversion is performed without operating the CPU (the Snooze mode).

- When using the Snooze mode function, set AWC to 1 in hardware trigger wait mode.
- Using the Snooze mode function in the software trigger no-wait mode, software trigger wait mode, or hardware trigger no-wait mode is prohibited.
- Using the Snooze mode function in the sequential conversion mode and hardware trigger wait mode is prohibited.
- When using the Snooze mode function, specify a hardware trigger interval of at least "shift time to Snooze mode*1 + conversion start time + A/D power supply stabilization wait time + A/D conversion time + 2 PCLKB clock cycles + 5 µs".
- Even when using Snooze mode, be sure to set the AWC bit to 0 in normal operation and change it to 1 just before shifting to Software Standby mode.
  Also, be sure to change the AWC bit to 0 after returning from Software Standby mode to normal operation.
  If the AWC bit is left set to 1, A/D conversion will not start normally in spite of the subsequent Snooze mode or normal operation.

Note 1. Refer to Table 31.21 in section 31.4.2. Wakeup Time.

[Before correction of 25.2.6 ADS: Analog Input Channel Specification Register] (Page 578)

(Omitted)

Note: Rewrite the value of the ADISS bit while conversion is stopped (ADCS = 0, ADCE = 0).

Note: If using VREFH0 as the '+' side reference voltage of the A/D converter, do not select AN000 as an A/D conversion channel.

Note: If using VREFL0 as the '-' side reference voltage of the A/D converter, do not select AN001 as an A/D conversion channel.

Note: When the setting of the ADISS bit is 1, the internal reference voltage cannot be used for the '+' side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see section 25.6.5. Example of Using the ADC12 when Selecting the Temperature Sensor Output Voltage or Internal Reference Voltage, and Software Trigger No-wait Mode and One-shot Conversion Mode.

For details about the internal reference voltage, see section 31, Electrical Characteristics T_A = -40 to +105°C.

Note: Do not set the ADISS bit to 1 when shifting to Software Standby mode, or to Sleep mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in section 31.3.2. Operating and Standby Current will be added.

Note: When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used at the same time.

[After correction of 25.2.6 ADS: Analog Input Channel Specification Register]

(Omitted)

Note: Rewrite the value of the ADISS bit while conversion is stopped (ADCS = 0, ADCE = 0).

Note: If using VREFH0 as the '+' side reference voltage of the A/D converter, do not select AN000 as an A/D conversion channel.

Note: If using VREFL0 as the '-' side reference voltage of the A/D converter, do not select AN001 as an A/D conversion channel.

Note: When the setting of the ADISS bit is 1, the internal reference voltage cannot be used for the '+' side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see section 25.6.5. Example of Using the ADC12 when Selecting the Temperature Sensor Output Voltage or Internal Reference Voltage, and Software Trigger No-wait Mode and One-shot Conversion Mode.

For details about the internal reference voltage, see section 31, Electrical Characteristics T_A = -40 to +105°C.

Note: Do not set the ADISS bit to 1 when shifting to Software Standby mode, or to Sleep mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in section 31.3.2. Operating and Standby Current will be added.

Note: When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used at the same time.

Note: When the setting of the ADISS bit is 1, the software trigger wait mode and one-shot conversion mode cannot be used at the same time.

[Before correction of Figure 25.13 Example of software trigger wait mode (select mode, one-shot conversion mode) operation timing] (Page 587)

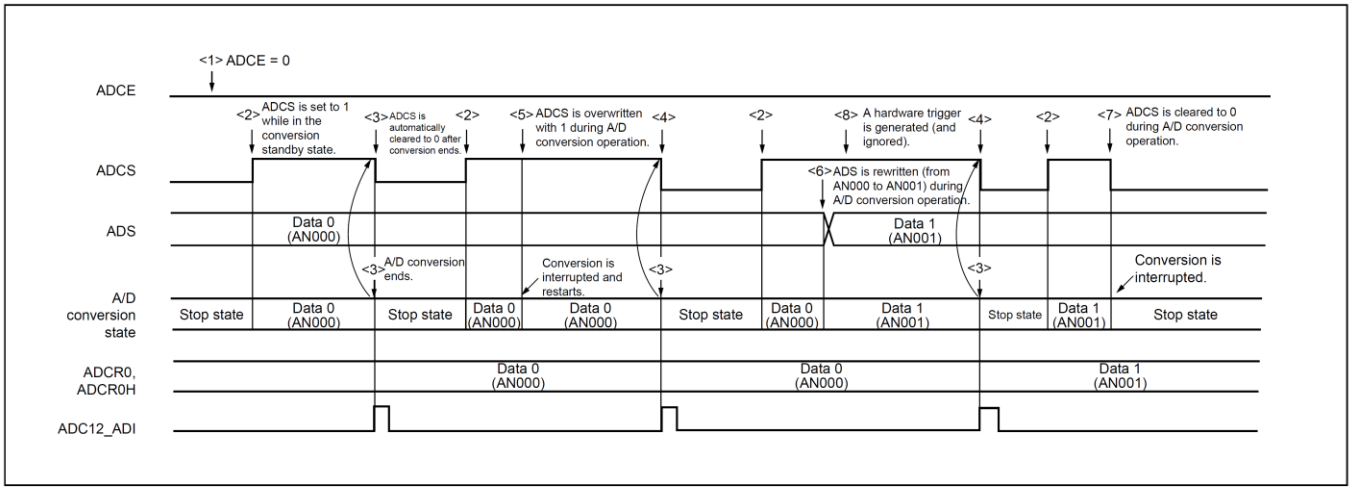


Figure 25.13 Example of software trigger wait mode (select mode, one-shot conversion mode) operation timing

Note: When <5> or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (f_{AD}). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See section 25.2.1. ADM0 : A/D Converter Mode Register 0 and section 25.2.1. ADM0 : A/D Converter Mode Register 0.)

[After correction of Figure 25.13 Example of software trigger wait mode (select mode, one-shot conversion mode) operation timing]

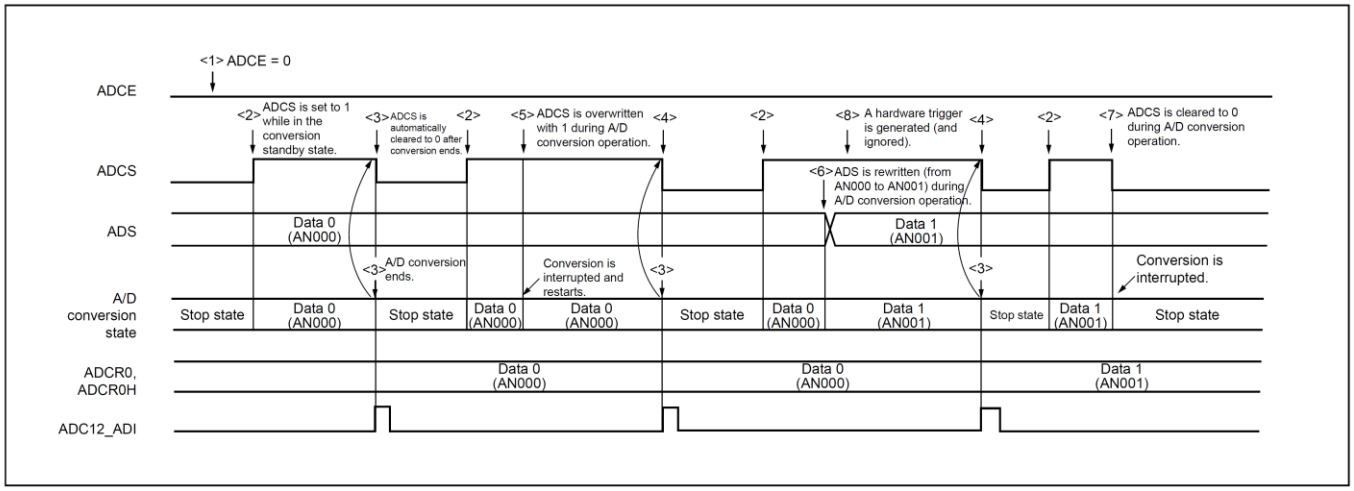


Figure 25.13 Example of software trigger wait mode (select mode, one-shot conversion mode) operation timing

Note: When <5> or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (f_{AD}). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See section 25.2.1. ADM0 : A/D Converter Mode Register 0 and section 25.2.1. ADM0 : A/D Converter Mode Register 0.)

Note: In software trigger wait mode (select mode, one-shot conversion mode), the ADISS = 1 setting (input source = temperature sensor output voltage, internal reference voltage) cannot be used.

[Before correction of 25.7 Snooze Mode Function] (Page 605)

25.7 Snooze Mode Function

In Snooze mode, A/D conversion is triggered by inputting a software trigger or a hardware trigger in the Software Standby mode. Normally, A/D conversion is stopped while in the Software Standby mode, but, by using the Snooze mode function, A/D conversion can be performed without operating the CPU. This is effective for reducing the operating current.

[After correction of 25.7 Snooze Mode Function]

25.7 Snooze Mode Function

In Snooze mode, A/D conversion is triggered by inputting a hardware trigger in the Software Standby mode.
Normally, A/D conversion is stopped while in the Software Standby mode, but, by using the Snooze mode function, A/D conversion can be performed without operating the CPU. This is effective for reducing the operating current.

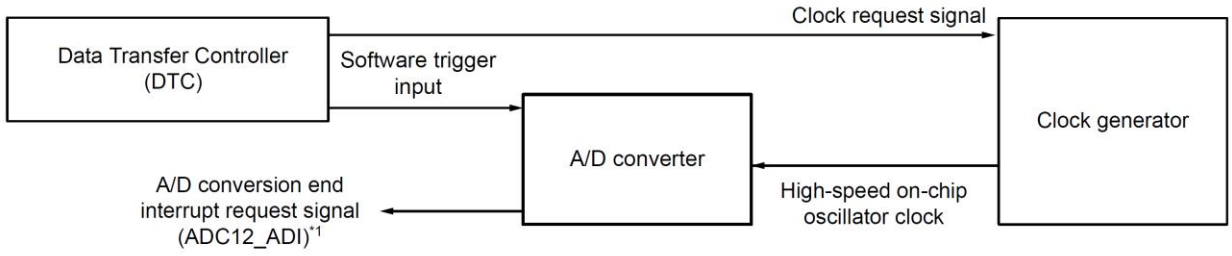
[Before correction of 25.7.1 A/D Conversion by Inputting a Software Trigger] (Page 605, Page 606)

25.7.1 A/D Conversion by Inputting a Software Trigger

In the Snooze mode, A/D conversion is triggered by inputting a software trigger. A software trigger generated by the DTC is used as an input trigger for A/D conversion. When performing A/D conversion by inputting a software trigger in Snooze mode, only the following four conversion modes can be used.

- Software trigger wait mode (select mode, one-shot conversion mode)
- Software trigger wait mode (select mode, sequential conversion mode)
- Software trigger wait mode (scan mode, one-shot conversion mode)
- Software trigger wait mode (scan mode, sequential conversion mode)

Note: The Snooze mode can only be specified when the high-speed on-chip oscillator clock or medium-speed on-chip oscillator clock is selected for PCLKB.



Note 1. Clear the setting of the A/D conversion result comparison function (ADRCK bit and ADUL/ADLL register) to the initial value so that an interrupt signal is generated each time conversion is completed.
- One-shot conversion mode (select/scan)
  When the Software Standby instruction is executed after the A/D conversion is completed and the interrupt request signal (ADC12_ADI) is generated, the supplied clock can be stopped.
- Sequential conversion mode (select/scan)
  When ADCS is written with 0 after the A/D conversion is completed and the interrupt request signal (ADC12_ADI) is generated, the sequential conversion mode is stopped. After that, when the Software Standby instruction is executed after 2 cycles of the conversion clock (f_{AD}) have elapsed, the supplied clock can be stopped.

Figure 25.24 Block diagram when using Snooze mode in software trigger wait mode

When using the Snooze mode, the initial setting of each register is specified before switching to the Software Standby mode (for details about these settings, see section 25.6.2. Setting up Software Trigger Wait Mode). If a software trigger (ADCS = 1) is input after switching to the Software Standby mode, the high-speed on-chip oscillator clock is supplied to the A/D converter. After supplying this clock, the A/D converter automatically counts up to the A/D power supply stabilization wait time, and then A/D conversion starts.

Table 25.20 Setting up software trigger no-wait mode

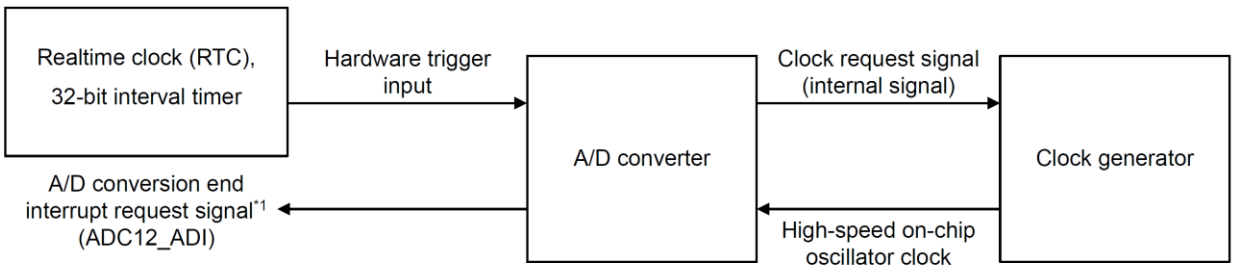
Step		Process	Detail
Normal operation	<1>	MSTPCRD register setting	The ADC bit of the MSTPCRD register is set to 0, and supplying the clock starts.
	<2>	PmnPFS_A register settings	The ports are set as the analog input. (See section 16.5.4. Notes on Using Analog Functions.)
	<3>	• ADM0 register setting • ADM1 register setting • ADM2 register setting • ADUL and ADLL register setting • ADS register setting (The order of the settings is irrelevant.)	• ADM0 register FR[2:0], LV[1:0]: bits: These are used to specify the A/D conversion time. ADMD bit: Select mode or scan mode • ADM1 register ADTMD1 and ADTMD0 bits: These are used to specify the software trigger wait mode. ADSCM bit: One-shot conversion mode • ADM2 register ADREFP[1:0], and ADREFM bits: These are used to select the reference voltage. ADRCK bit: This is used to select the range for the A/D conversion result comparison value for generating the interrupt signal from AREA1, AREA3, and AREA 2. ADTYP[1:0] bits: 12-bit, 10-bit, or 8-bit resolution • ADUL and ADLL register These are used to specify the upper limit and lower limit A/D conversion result comparison values. • ADS register ADS[4:0] bits: These are used to select the analog input channels.
	<4>	Reference voltage stabilization wait time count A	The reference voltage stabilization wait time count indicated by A below may be required if the values of the ADREFP[1:0] bits are changed. If the values of ADREFP[1:0] are changed to 10b, respectively: A = 5 µs Before changing as above, perform reference supply discharge (1 µs) by setting ADREFP[1:0] = 11b. A wait is not required if the values of ADREFP[1:0] are changed to 00b or 01b, respectively.
Software Standby mode	<5>	Enter the Software Standby mode	Leave the AWC and ADCE bits at the initial value 0. These bits are not re-set.
Snooze mode	<6>	Software trigger generation	After software trigger (ADCS = 1) is generated, the A/D converter automatically counts up to the A/D power supply stabilization wait time and A/D conversion is started in Snooze mode.
		⋮	(The A/D conversion operations are performed)
	<7>	End of A/D conversion	—
	<8>	ADC12_ADI generation*2	The A/D conversion end interrupt (ADC12_ADI) is generated.*1
	<9>	Storage of conversion results in the ADCRn or ADCRnH register	The conversion results are stored in the ADCRn or ADCRnH register.
	<10>	End processing*3	—
Software Standby mode	<11>	Software Standby instruction available*4	—

Note 1. Depending on the settings of the ADRCK bit, ADUL and ADLL registers, there is a possibility of no interrupt signal being generated. In this case, the results are not stored in the ADCRn or ADCRnH register.
Note 2. Clear the ADRCK bit, ADUL and ADLL registers to the initial value in the initial setting, and specify settings so that an interrupt request signal (ADC12_ADI) is generated each time A/D conversion is completed.
Note 3. Sequential conversion mode requires the end processing. Write 0 to ADCS after ADC12_ADI is generated. Then, after 2 cycles of the conversion clock (f_{AD}) have elapsed, the Software Standby instruction can be executed.
Note 4. If a software trigger is input after the Software Standby instruction, A/D conversion operation is again performed in the Snooze mode.

[After correction of 25.7.1 A/D Conversion by Inputting a Software Trigger]

All deleted.

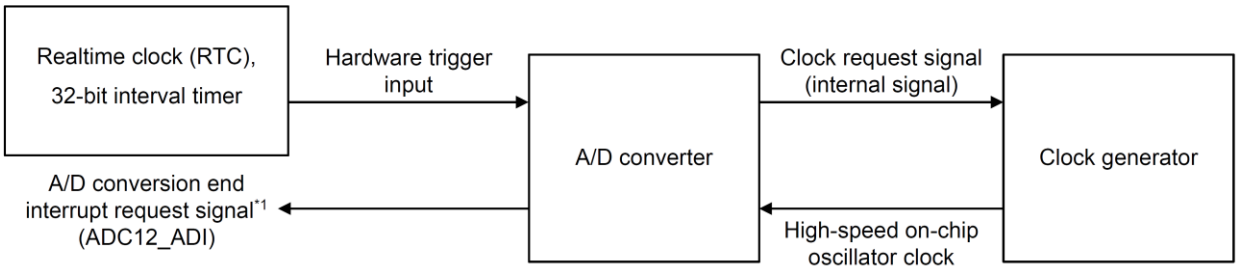
[Before correction of Figure 25.25 Block diagram when using Snooze mode in hardware trigger wait mode] (Page 607)



Note 1. Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.
When the 32-bit interval timer interrupt signal (ADITL0 (= TML32_ITL0)) is selected as a hardware trigger, the detection flag in the ITLS0 register has to be cleared each time a 32-bit interval timer interrupt signal (ADITL0 (= TML32_ITL0)) is generated.
Therefore, clear the setting of the A/D conversion result comparison function (ADRCK bit and ADUL/ADLL register) to the initial value so that an A/D conversion end interrupt request signal (ADC12_ADI) is generated upon completion of A/D conversion.

Figure 25.25 Block diagram when using Snooze mode in hardware trigger wait mode

[After correction of Figure 25.25 Block diagram when using Snooze mode in hardware trigger wait mode]



Note 1. Depending on the setting of the A/D conversion result comparison function (ADRCK bit, ADUL/ADLL register), there is a possibility of no interrupt signal being generated.

Figure 25.25 Block diagram when using Snooze mode in hardware trigger wait mode

[Before correction of Table 28.5 Mapping for the extra bit of the startup area selection and security setting (address (P/E) :0x0000_0010)] (Page 633)

Table 28.5 Mapping for the extra bit of the startup area selection and security setting (address (P/E) : 0x0000_0010)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SASMF*1	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

Note 1. Once 0 is set for these bits, it cannot be changed to 1.

[After correction of Table 28.5 Mapping for the extra bit of the startup area selection and security setting (address (P/E) :0x0000_0010)]

Table 28.5 Mapping for the extra bit of the startup area selection and security setting (address (P/E) : 0x0000_0010)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
BTFLG	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

Note 1. Once 0 is set for these bits, it cannot be changed to 1.

[Before correction of Table 28.6 Mapping for the extra bit of the access window information program (address (P/E) :0x0000_0010)] (Page 633)

Table 28.6 Mapping for the extra bit of the access window information program (address (P/E) : 0x0000_0010)

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
SASMF*1	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

Note 1. Once 0 is set as data in these bits, it cannot be changed to 1.

[After correction of Table 28.6 Mapping for the extra bit of the access window information program (address (P/E) :0x0000_0010)]

Table 28.6 Mapping for the extra bit of the access window information program (address (P/E) : 0x0000_0010)

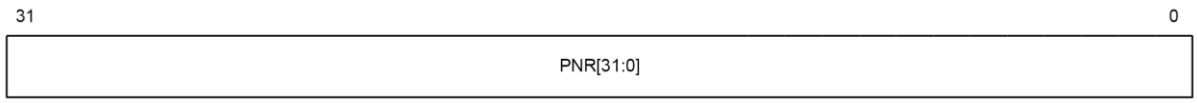
b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
BTFLG	—	—	—	—	FAWE[10:0]										
b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FSPR*1	—	—	—	—	FAWS[10:0]										

Note 1. Once 0 is set as data in these bits, it cannot be changed to 1.

[Before correction of 28.3.25 PNRn : Part Numbering Register n (n = 0 to 3)] (Page 641)

28.3.25 PNRn : Part Numbering Register n (n = 0 to 3)

Address: 0x0101_1080 + n × 4



Value after reset: Unique value for each chip

Bit	Symbol	Function	R/W
31:0	PNR[31:0]	Part Number	R

The PNRn is a read-only register that stores a 16-byte part numbering. The PNRn register should be read in 32-bit units.

Each byte corresponds to the ASCII code representation of the product part number as detailed in product list.

In case of the part number is ’R7FA0E1073CNK’, 16-byte part numbering is stored as follows.

Address 0x0101_1080: ’K’, 0x4B in ASCII code

Address 0x0101_1081: ’N’, 0x4E in ASCII code

Address 0x0101_1082: ’C’, 0x43 in ASCII code

Address 0x0101_1083: ’3’, 0x33 in ASCII code

Address 0x0101_1084: ’7’, 0x37 in ASCII code

Address 0x0101_1085: ’0’, 0x30 in ASCII code

Address 0x0101_1086: ’1’, 0x31 in ASCII code

Address 0x0101_1087: ’E’, 0x45 in ASCII code

Address 0x0101_1088: ’0’, 0x30 in ASCII code

Address 0x0101_1089: ’A’, 0x41 in ASCII code

Address 0x0101_1090: ’F’, 0x46 in ASCII code

Address 0x0101_1091: ’7’, 0x37 in ASCII code

Address 0x0101_1092: ’R’, 0x52 in ASCII code

Address 0x0101_1093: ’’ (space) , 0x20 in ASCII code

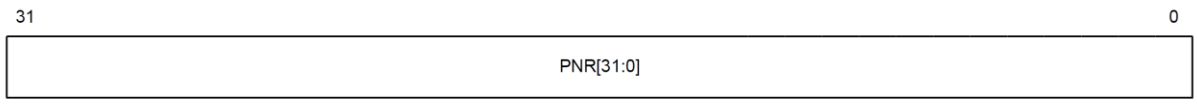
Address 0x0101_1094: ’’ (space) , 0x20 in ASCII code

Address 0x0101_1095: ’’ (space) , 0x20 in ASCII code

[After correction of 28.3.25 PNRn : Part Numbering Register n (n = 0 to 3)]

28.3.25 PNRn : Part Numbering Register n (n = 0 to 3)

Address: 0x0101_1080 + n × 4



Value after reset: Unique value for each chip

Bit	Symbol	Function	R/W
31:0	PNR[31:0]	Part Number	R

The PNRn is a read-only register that stores a 16-byte part numbering. The PNRn register should be read in 32-bit units.

Each byte corresponds to the ASCII code representation of the product part number as detailed in product list.

In case of the part number is ’R7FA0E1073CNK’, 16-byte part numbering is stored as follows.

Address 0x0101_1080: ’K’, 0x4B in ASCII code

Address 0x0101_1081: ’N’, 0x4E in ASCII code

Address 0x0101_1082: ’C’, 0x43 in ASCII code

Address 0x0101_1083: ’3’, 0x33 in ASCII code

Address 0x0101_1084: ’7’, 0x37 in ASCII code

Address 0x0101_1085: ’0’, 0x30 in ASCII code

Address 0x0101_1086: ’1’, 0x31 in ASCII code

Address 0x0101_1087: ’E’, 0x45 in ASCII code

Address 0x0101_1088: ’0’, 0x30 in ASCII code

Address 0x0101_1089: ’A’, 0x41 in ASCII code

Address 0x0101_108A: ’F’, 0x46 in ASCII code

Address 0x0101_108B: ’7’, 0x37 in ASCII code

Address 0x0101_108C: ’R’, 0x52 in ASCII code

Address 0x0101_108D: ’’ (space) , 0x20 in ASCII code

Address 0x0101_108E: ’’ (space) , 0x20 in ASCII code

Address 0x0101_108F: ’’ (space) , 0x20 in ASCII code

[Before correction of Table 28.15 Basic functions] (Page 644)

Table 28.15 Basic functions

Function	Functional overview	Availability
		Self-programming/SWD programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded.	Supported
Block erasure	Erases the memory contents in the specified block	Supported
Programming	Writes to the specified address	Supported
Read	Reads data programmed in the flash memory	Not supported (read by user program is possible)
ID code protection	Compares the ID code sent by the host with the code stored in the code flash memory. If the two match, the FCB enters the wait state for programming and erasure commands from the host.	Not supported (ID authentication is not performed)
Protection configuration	Configures the access window for flash area protection in the code flash memory	Supported

[After correction of Table 28.15 Basic functions]

Table 28.15 Basic functions

Function	Functional overview	Availability	
		Self-programming	SWD programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded.	Supported	Supported
Block erasure	Erases the memory contents in the specified block	Supported	Supported
Programming	Writes to the specified address	Supported	Supported
Read	Reads data programmed in the flash memory	Not supported (read by user program is possible)	Not supported
ID code check	Compares the ID code sent by the host with the code stored in the code flash memory. If the two match, the FCB enters the wait state for programming and erasure commands from the host.	Not supported (ID authentication is not performed)	Supported
Security configuration	Configures the protection of security function (Access window and Start-up area selection	Supported with conditions See section 28.8. Protection	Supported with conditions See section 28.8. Protection
Protection configuration	Configures the access window for flash area protection in the code flash memory	Supported	Supported

[Before correction of 29 True Random Number Generator (TRNG)] (Page 666)

29.3 Operation

29.3.1 Overall Processing Flow

Table 29.2 shows the overall processing flow of TRNG activation.

Table 29.2 Procedure for using the True Random Number Generator to generate a random number seed

No	Step Name	Description
1	Module stop setting	Set the MSTPCRC.MSTPC28 = 0 to cancel the module-stop state.
2	Wait	Wait for the peripheral module clock (PCLKB) × 6.
3	TRNG enable setting	Set the TRNGSCR0.SGCEN = 1 to enable the true random number generator.
4	TRNG interrupt setting	Set the TRNGSCR1.INTEN bit to enable/disable the TRNG interrupt output.
5	TRNG operation start setting	Set the TRNGSCR0.SGSTART = 1 to start the generation of a random number seed.
6	Read the seed data	There are 2 operation for TRNG seed generation, Polling and Interrupt. 1. Polling operation ; Read TRNGSDR for 4 times after the TRNGSCR0.RDRDY = 1 2. Interrupt operation ; Read TRNGSDR register for 4 times after TRNG interrupt is generated.
7	TRNG operation stop setting	Set the TRNGSCR0.SGCEN = 0 to disable the true random number generator. Set the TRNGSCR0.SGSTART = 0 to stop the generation of a random number seed.
8	Module stop setting	Set the MSTPCRC.MSTPC28 = 1 to enter the module-stop state.

[After correction of 29 True Random Number Generator (TRNG)]

29.3 Operation

29.3.1 Overall Processing Flow

Table 29.2 shows the overall processing flow of TRNG activation.

Table 29.2 Procedure for using the True Random Number Generator to generate a random number seed

No	Step Name	Description
1	Module stop setting	Set the MSTPCRC.MSTPC28 = 0 to cancel the module-stop state.
2	Wait	Wait for the peripheral module clock (PCLKB) × 6.
3	TRNG enable setting	Set the TRNGSCR0.SGCEN = 1 to enable the true random number generator.
4	TRNG interrupt setting	Set the TRNGSCR1.INTEN bit to enable/disable the TRNG interrupt output.
5	TRNG operation start setting	Set the TRNGSCR0.SGSTART = 1 to start the generation of a random number seed.
6	Read the seed data	There are 2 operation for TRNG seed generation, Polling and Interrupt. 1. Polling operation ; Read TRNGSDR for 4 times after the TRNGSCR0.RDRDY = 1 2. Interrupt operation ; Read TRNGSDR register for 4 times after TRNG interrupt is generated.
7	TRNG operation stop setting	Set the TRNGSCR0.SGCEN = 0 to disable the true random number generator. Set the TRNGSCR0.SGSTART = 0 to stop the generation of a random number seed.
8	Module stop setting	Set the MSTPCRC.MSTPC28 = 1 to enter the module-stop state.

29.4 Usage Notes

TRNG operation is prohibited for a period of 20 µs before and after the MCU operation mode transition.

[Before correction of Table 31.1 Absolute maximum ratings] (Page 668)

Table 31.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
VCL pin input voltage		V_{IVCL}	-0.3 to +2.1 and -0.3 to VCC + 0.3*1	V
Input voltage	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407	V_I1	-0.3 to VCC + 0.3	V
	P913, P914 (5 V tolerant)	V_I2	-0.3 to +6.5	V
	P008 to P015, P212 to P215	V_I3	-0.3 to VCC + 0.3	V
Output voltage	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	V_O1	-0.3 to VCC + 0.3	V
	P913, P914 (N-ch open-drain)	V_O2	-0.3 to +6.5	V
	P008 to P015, P212, P213	V_O3	-0.3 to VCC + 0.3*2	V

Table 31.1 Absolute maximum ratings (2 of 2)

Parameter			Symbol	Value	Unit
Analog input voltage	AN000 to AN007		$V_{AI}1$	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3*2 *3	V
	AN021 to AN022		$V_{AI}2$	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3*2 *3	V
High-level output current	P100 to P103, P108 to P110, P112, P201 to P207, P208, P300, P407	Per pin	$I_{OH}1$	-40	mA
		Total of all pins		-100	mA
	P008 to P015, P212, P213	Per pin	$I_{OH}2$	-5	mA
		Total of all pins		-20	mA
Low-level output current	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407, P913, P914	Per pin	$I_{OL}1$	40	mA
		Total of all pins		100	mA
	P008 to P015, P212, P213	Per pin	$I_{OL}2$	10	mA
		Total of all pins		20	mA
Ambient operating temperature	In normal operation mode		Ta	-40 to +105	°C
	In flash memory programming mode			-40 to +105	°C
Storage temperature			Tstg	-65 to +150	°C

Note 1. Connect the VCL pin to VSS via a capacitor (0.47 to 1 µF). The listed value is the absolute maximum rating of the VCL pins. Only use the capacitor connection. Do not apply a specific voltage to this pin.
Note 2. This voltage must be no higher than 6.5 V.
Note 3. The voltage on a pin in use for A/D conversion must not exceed VREFH0 + 0.3.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note: VREFH0 refers to the positive reference voltage of the A/D converter.

Note: The reference voltage is VSS.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

[After correction of Table 31.1 Absolute maximum ratings]

Table 31.1 Absolute maximum ratings (1 of 2)

Parameter		Symbol	Value	Unit
Power supply voltage		VCC	-0.5 to +6.5	V
VCL pin input voltage		V_{IVCL}	-0.3 to +2.1 and -0.3 to VCC + 0.3*1	V
Input voltage	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407	V_I1	-0.3 to VCC + 0.3*2	V
	P913, P914 (5 V tolerant)	V_I2	-0.3 to +6.5	V
	P008 to P015, P212 to P215	V_I3	-0.3 to VCC + 0.3*2	V
Output voltage	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407	V_O1	-0.3 to VCC + 0.3*2	V
	P913, P914 (N-ch open-drain)	V_O2	-0.3 to +6.5	V
	P008 to P015, P212, P213	V_O3	-0.3 to VCC + 0.3*2	V

Table 31.1 Absolute maximum ratings (2 of 2)

Parameter			Symbol	Value	Unit
Analog input voltage	AN000 to AN007		$V_{AI}1$	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3*2 *3	V
	AN021 to AN022		$V_{AI}2$	-0.3 to VCC + 0.3 and -0.3 to VREFH0 + 0.3*2 *3	V
High-level output current	P100 to P103, P108 to P110, P112, P201 to P207, P208, P300, P407	Per pin	$I_{OH}1$	-40	mA
		Total of all pins		-100	mA
	P008 to P015, P212, P213	Per pin	$I_{OH}2$	-5	mA
		Total of all pins		-20	mA
Low-level output current	P100 to P103, P108 to P110, P112, P201, P206 to P208, P300, P407, P913, P914	Per pin	$I_{OL}1$	40	mA
		Total of all pins		100	mA
	P008 to P015, P212, P213	Per pin	$I_{OL}2$	10	mA
		Total of all pins		20	mA
Ambient operating temperature	In normal operation mode		Ta	-40 to +105	°C
	In flash memory programming mode			-40 to +105	°C
Storage temperature			Tstg	-65 to +150	°C

Note 1. Connect the VCL pin to VSS via a capacitor (0.47 to 1 µF). The listed value is the absolute maximum rating of the VCL pins. Only use the capacitor connection. Do not apply a specific voltage to this pin.
Note 2. This voltage must be no higher than 6.5 V.
Note 3. The voltage on a pin in use for A/D conversion must not exceed VREFH0 + 0.3.

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note: VREFH0 refers to the positive reference voltage of the A/D converter.

Note: The reference voltage is VSS.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

[Before correction of Table 31.11 I/O other characteristics] (Page 674, Page 675)

Table 31.11 I/O other characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current, high	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407, P913, P914	$I_{LIH}1$	—	—	1	µA	V_I = VCC
	P008 to P015	$I_{LIH}2$	—	—	1	µA	V_I = VCC
	P212 to P214	$I_{LIH}3$	—	—	1	µA	V_I = VCC

Table 31.11 I/O other characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current, low	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407, P913, P914	$I_{LIL}1$	—	—	-1	µA	V_I = VSS
	P008 to P015	$I_{LIL}2$	—	—	-1	µA	V_I = VSS
	P212 to P214	$I_{LIL}3$	—	—	-1	µA	V_I = VSS
On-chip pll-up resistance	P100 to P103, P108 to P110, P112, P201, P206 to P208, P212, P213, P300, P407	R_U	10	20	100	kΩ	V_I = VSS In input port
Input capacitance	P200	Cin	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	Other input pins		—	—	15		

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

[After correction of Table 31.11 I/O other characteristics]

Table 31.11 I/O other characteristics (1 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current, high	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407, P913, P914	$I_{LIH}1$	—	—	1	µA	V_I = VCC
	P008 to P015	$I_{LIH}2$	—	—	1	µA	V_I = VCC
	P212 to P215	$I_{LIH}3$	—	—	1	µA	V_I = VCC

Table 31.11 I/O other characteristics (2 of 2)

Conditions: VCC = 1.6 to 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current, low	P100 to P103, P108 to P110, P112, P200, P201, P206 to P208, P300, P407, P913, P914	$I_{LIL}1$	—	—	-1	µA	V_I = VSS
	P008 to P015	$I_{LIL}2$	—	—	-1	µA	V_I = VSS
	P212 to P215	$I_{LIL}3$	—	—	-1	µA	V_I = VSS
On-chip pll-up resistance	P100 to P103, P108 to P110, P112, P201, P206 to P208, P212, P213, P300, P407	R_U	10	20	100	kΩ	V_I = VSS In input port
Input capacitance	P200	Cin	—	—	30	pF	Vin = 0 V, f = 1 MHz, Ta = 25°C
	Other input pins		—	—	15		

Note: The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

[Before correction of Table 31.12 Operating and standby current (1) (2 of 2)] (Page 677)

Table 31.12 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter						Symbol	Typ*5	Max	Unit	Test Conditions
Supply current*1	Subosc-speed mode*4	Normal mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C	Icc	3.3	—	µA	—
					Ta = 25°C		3.7	—		
					Ta = 50°C		3.9	—		
					Ta = 70°C		4.3	—		
					Ta = 85°C		4.8	—		
					Ta = 105°C		6.2	—		
			Peripheral clocks enabled*6	ICLK = 32.768 kHz	Ta = -40°C		—	7.2		
					Ta = 25°C		—	7.9		
					Ta = 50°C		—	9.6		
					Ta = 70°C		—	13.0		
					Ta = 85°C		—	18.8		
					Ta = 105°C		—	36.5		
		Sleep mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C		1.0	—		—
					Ta = 25°C		1.3	—		
					Ta = 50°C		1.5	—		
					Ta = 70°C		1.8	—		
					Ta = 85°C		2.2	—		
					Ta = 105°C		3.2	—		
			Peripheral clocks enabled*6	ICLK = 32.768 kHz	Ta = -40°C		—	4.8		
					Ta = 25°C		—	5.4		
					Ta = 50°C		—	7.0		
					Ta = 70°C		—	10.5		
					Ta = 85°C		—	16.1		
					Ta = 105°C		—	33.3		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.

Note 2. The clock source is high-speed on-chip oscillator (HOCO).

Note 3. The clock source is middle-speed on-chip oscillator (MOCO).

Note 4. The clock source is the Sub-clock oscillator (SOSC) and CMC.SODRV[1:0] are 10b (Low power mode 2).

Note 5. VCC = 3.3 V.

Note 6. Includes operating current for PCLBUZ, TAU, SAU, and IICA functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 31.14.

[After correction of Table 31.12 Operating and standby current (1) (2 of 2)]

Table 31.12 Operating and standby current (1) (2 of 2)

Conditions: VCC = 1.6 to 5.5 V

Parameter						Symbol	Typ*5	Max	Unit	Test Conditions
Supply current*1	Subosc-speed mode*4	Normal mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C	Icc	3.3	—	µA	—
					Ta = 25°C		3.7	—		
					Ta = 50°C		3.9	—		
					Ta = 70°C		4.3	—		
					Ta = 85°C		4.8	—		
					Ta = 105°C		6.2	—		
			Peripheral clocks enabled*7	ICLK = 32.768 kHz	Ta = -40°C		—	7.2		
					Ta = 25°C		—	7.9		
					Ta = 50°C		—	9.6		
					Ta = 70°C		—	13.0		
					Ta = 85°C		—	18.8		
					Ta = 105°C		—	36.5		
		Sleep mode	Peripheral clocks disabled	ICLK = 32.768 kHz	Ta = -40°C		1.0	—		—
					Ta = 25°C		1.3	—		
					Ta = 50°C		1.5	—		
					Ta = 70°C		1.8	—		
					Ta = 85°C		2.2	—		
					Ta = 105°C		3.2	—		
			Peripheral clocks enabled*7	ICLK = 32.768 kHz	Ta = -40°C		—	4.8		
					Ta = 25°C		—	5.4		
					Ta = 50°C		—	7.0		
					Ta = 70°C		—	10.5		
					Ta = 85°C		—	16.1		
					Ta = 105°C		—	33.3		

Note 1. Supply current is the total current flowing into VCC. Supply current values apply when internal pull-up MOSs are in the off state and these values do not include output charge/discharge current from any of the pins.

Note 2. The clock source is high-speed on-chip oscillator (HOCO).

Note 3. The clock source is middle-speed on-chip oscillator (MOCO).

Note 4. The clock source is the Sub-clock oscillator (SOSC) and CMC.SODRV[1:0] are 10b (Low power mode 2).

Note 5. VCC = 3.3 V.

Note 6. Includes operating current for PCLBUZ, TAU, SAU, and IICA functions only. For other peripheral operating currents, please add the current in Peripheral Functions Supply current in Table 31.14.

Note 7. Includes operating current for PCLBUZ, TAU and SAU functions only. For other peripheral operating currents, please add the current in Table 31.14.

[Before correction of Table 31.16 Reset timing (2 of 2)] (Page 684)

Table 31.16 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after internal reset cancellation (Independent watchdog timer reset, SRAM parity error reset, software reset)	t_{RESWT3}	—	0.04	0.041	ms	—

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. When RES pin is not used as the external reset input, this specification can be ignore.

[After correction of Table 31.16 Reset timing (2 of 2)]

Table 31.16 Reset timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Internal reset by independent watch dog timer reset, SRAM parity error reset, software reset	t_{RESW2}	—	0.04	0.041	ms	—

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.
Note 3. When RES pin is not used as the external reset input, this specification can be ignore.

[Before correction of Figure 31.11 Reset input timing (2)] (Page 684)

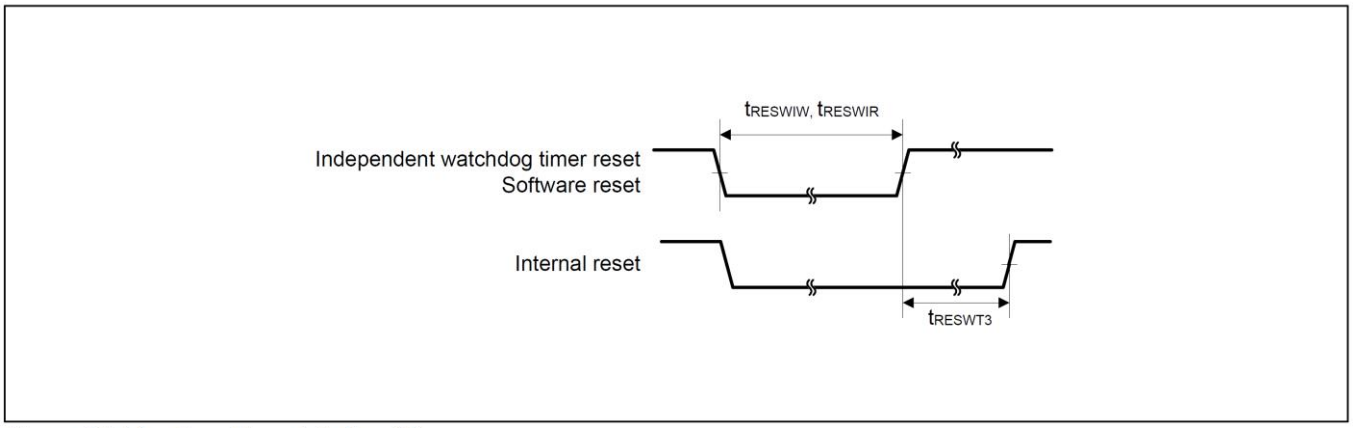
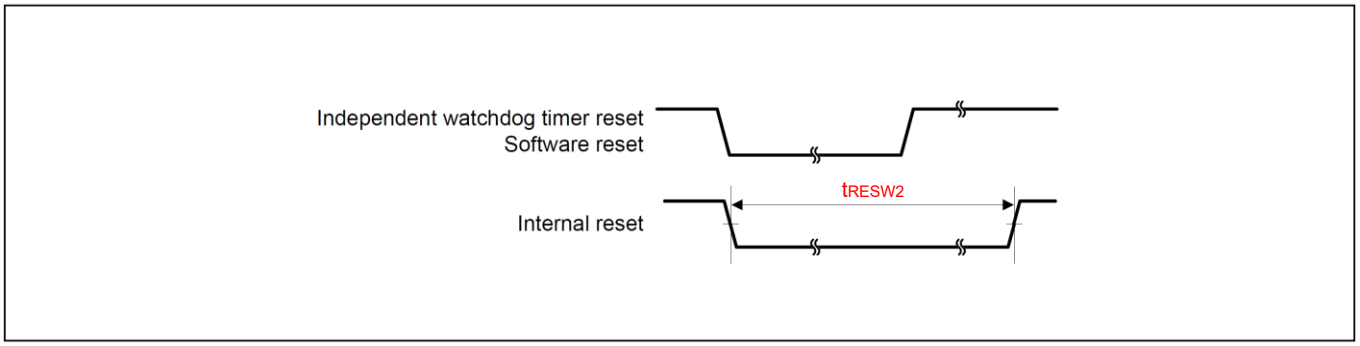


Figure 31.11 Reset input timing (2)

[After correction of Figure 31.11 Reset input timing (2)]



[Before correction of Table 31.46 LVD1 characteristics (2 of 2)] (Page 719)

Table 31.46 LVD1 characteristics (2 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_B}	2.25	2.30	2.34	V	The power supply voltage is rising.
			2.20	2.25	2.29	V	The power supply voltage is falling.
		V_{det1_C}	2.15	2.20	2.24	V	The power supply voltage is rising.
			2.10	2.15	2.19	V	The power supply voltage is falling.
		V_{det1_D}	2.05	2.09	2.13	V	The power supply voltage is rising.
			2.00	2.04	2.08	V	The power supply voltage is falling.
		V_{det1_E}	1.94	1.98	2.02	V	The power supply voltage is rising.
			1.90	1.94	1.98	V	The power supply voltage is falling.
		V_{det1_F}	1.84	1.88	1.91	V	The power supply voltage is rising.
			1.80	1.84	1.87	V	The power supply voltage is falling.
		V_{det1_10}	1.74	1.78	1.81	V	The power supply voltage is rising.
			1.70	1.74	1.77	V	The power supply voltage is falling.
		V_{det1_11}	1.64	1.67	1.70	V	The power supply voltage is rising.
			1.60	1.63	1.66	V	The power supply voltage is falling.
Minimum pulse width		t_{LW}	500	—	—	µs	—
Detection delay time		—	—	—	500	µs	—

[After correction of Table 31.46 LVD1 characteristics (2 of 2)]

Table 31.47 LVD1 characteristics (2 of 2)

Conditions: VPDR ≤ VCC ≤ 5.5 V, VSS = 0 V, Ta = -40 to +105°C

Parameter		Symbol	Min	Typ	Max	Unit	Test Conditions
Detection voltage	Supply voltage level	V_{det1_B}	2.25	2.30	2.34	V	The power supply voltage is rising.
			2.20	2.25	2.29	V	The power supply voltage is falling.
		V_{det1_C}	2.15	2.20	2.24	V	The power supply voltage is rising.
			2.10	2.15	2.19	V	The power supply voltage is falling.
		V_{det1_D}	2.05	2.09	2.13	V	The power supply voltage is rising.
			2.00	2.04	2.08	V	The power supply voltage is falling.
		V_{det1_E}	1.94	1.98	2.02	V	The power supply voltage is rising.
			1.90	1.94	1.98	V	The power supply voltage is falling.
		V_{det1_F}	1.84	1.88	1.91	V	The power supply voltage is rising.
			1.80	1.84	1.87	V	The power supply voltage is falling.
		V_{det1_10}	1.74	1.78	1.81	V	The power supply voltage is rising.
			1.70	1.74	1.77	V	The power supply voltage is falling.
		V_{det1_11}	1.64	1.67	1.70	V	The power supply voltage is rising.
			1.60	1.63	1.66	V	The power supply voltage is falling.
Minimum pulse width		t_{LW1}	500	—	—	µs	—
Detection delay time		t_{det1}	—	—	500	µs	—
LVD1 detection voltage stabilization time (after changing the LVD1 detection voltage)		$t_{d(E-A)}$	—	—	1500	µs	—