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Old Company Name in Catalogs and Other Documents

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RENESAS TECHNICAL UPDATE

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Product Category	MPU & MCU		Document No.	TN-R8C-A001B/E	Rev.	2.00
Title	R8C/32A Group, R8C/33A Group, R8C/35A Group, R8C/36A Group, R8C/38A Group, R8C/3GA Group, R8C/3JA Group Specification Change		Information Category	Technical Notification		
Applicable Product	R8C/32A Group, R8C/33A Group, R8C/35A Group, R8C/36A Group, R8C/38A Group, R8C/3GA Group, R8C/3JA Group	Lot No. --	Reference Document			

1. Information

Specifications in the R8C/32A Group, R8C/33A Group, R8C/35A Group, R8C/36A Group, R8C/38A Group, R8C/3GA Group, and R8C/3JA Group datasheet and hardware manual have been changed.

1.1 Changes

(1) Removed high-speed on-chip oscillator function
(2) Changed the flash memory suspend function specification
(3) Changed the flash memory suspend function's electrical characteristics

1.2 Applicable Documents

- R8C/32A Group Datasheet Rev.0.20 (REJ03B0229-0020)
- R8C/32A Group Hardware Manual Rev.0.20 (REJ09B0458-0020)
- R8C/33A Group Datasheet Rev.0.20 (REJ03B0228-0020)
- R8C/33A Group Hardware Manual Rev.0.20 (REJ09B0455-0020)
- R8C/35A Group Datasheet Rev.0.40 (REJ03B0225-0040)
- R8C/35A Group Hardware Manual Rev.0.40 (REJ09B0407-0040)
- R8C/36A Group Hardware Manual Rev.0.20 (REJ09B0480-0020)
- R8C/38A Group Hardware Manual Rev.0.10 (REJ09B0485-0010)
- R8C/3GA Group Hardware Manual Rev.0.20 (REJ09B0472-0020)
- R8C/3JA Group Hardware Manual Rev.1.00 (REJ09B0508-0100)

2. Specification Change

2.1 High-Speed On-Chip Oscillator Function Removed

The high-speed on-chip oscillator function has been removed. Do not select the high-speed on-chip oscillator clock for the CPU clock or peripheral function. Descriptions regarding the high-speed on-chip oscillator in the applicable documents shown in 1.2, other than descriptions in this technical update, are invalid.

2.1.1 Clock Generation Circuit Register Setting

2.1.1.1 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do not set the FRA00 bit to 1 (high-speed on-chip oscillator on) [refer to Figure 2.1].
(2) Do not set the FRA01 bit to 1 (high-speed on-chip oscillator selected for the fOCO clock) [refer to Figure 2.1]. The fOCO clock is used for timer RA.
(3) Do not set the FRA03 bit to 1 (fOCO-F divided by 128 selected for the fOCO128 clock) [refer to Figure 2.1]. The fOCO128 clock is used for timers RC and RD.

2.1.1.2 System Clock Control Register 3 (CM3)

(1) Do not set bits CM37 to CM36 to 10b (high-speed on-chip oscillator clock selected for the CPU clock when the MCU exits wait mode or stop mode) [refer to Figure 2.2].

2.1.1.3 High-Speed On-Chip Oscillator Cotrol Registers 1 to 7 (FRA1 to FRA7)

(1) Do not set the register related to the high-speed on-chip oscillator division select (FRA2) or registers related to the frequency adjustment (FRA1 and FRA3 to FRA7) .

2.1.2 Timer RA Register Setting

2.1.2.1 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do not set the FRA01 bit to 1 (high-speed on-chip oscillator selected for the fOCO clock) [refer to Figure 2.1]. The high-speed on-chip oscillator clock cannot be selected for the timer RA count source.

2.1.3 Timer RC Register Setting

2.1.3.1 Timer RC Control Register 1 (TRCCR1)

(1) Do not set bits TCK2 to TCK0 to 110b (fOCO40M selected for the timer RC count source) [refer to Figure 2.3].

(2) Do not set bits TCK2 to TCK0 to 111b (fOCO-F selected for the timer RC count source) [refer to Figure 2.3].

2.1.3.2 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do not set the FRA03 bit to 1 (fOCO-F divided by 128 selected for the fOCO128 clock) [refer to Figure 2.1]. For the timer RC input-capture function, fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRCGRA register.

2.1.4 Timer RD Register Setting (only for the R8C/35A Group, R8C/36A Group, R8C/38A Group, and R8C/3JA Group*)

* The R8C/32A Group, R8C/33A Group, and R8C/3GA Group are not equipped with timer RD.

2.1.4.1 Timer RD Control Register 0, 1 (TRDCR0, TRDCR1)

(1) Do not set bits TCK2 to TCK0 to 110b (fOCO40M selected for the timer RD count source) [refer to Figure 2.4].

(2) Do not set bits TCK2 to TCK0 to 111b (fOCO-F selected for the timer RD count source) [refer to Figure 2.4].

2.1.4.2 High-Speed On-Chip Oscillator Control Register 0 (FRA0)

(1) Do not set the FRA03 bit to 1 (fOCO-F divided by 128 selected for the fOCO128 clock) [refer to Figure 2.1]. For the timer RD input-capture function, fOCO-F divided by 128 cannot be selected for the input-capture trigger input of the TRDGRA0 register.

2.1.5 A/D Converter Register Setting

2.1.5.1 A/D Mode Register (ADMOD)

(1) Do not set the CKS2 bit to 1 (fOCO-F selected for the A/D converter operating clock source) [refer to Figure 2.5].

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Address	0023h							
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	FRA03	—	FRA01	FRA00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	0: High-speed on-chip oscillator off 1: ~~High-speed on-chip oscillator on~~ → Do not set.	R/W
b1	FRA01	High-speed on-chip oscillator select bit(1)	0: Low-speed on-chip oscillator selected(2) 1: ~~High-speed on-chip oscillator selected~~ → Do not set.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	FRA03	fOCO128 clock select bit	0: fOCO-S divided by 128 selected 1: ~~fOCO-F divided by 128 selected~~ → Do not set.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

1. Change the FRA01 bit in the following conditions.
2. FRA00 = 1 (high-speed on-chip oscillator on)
3. The CM14 bit in the CM1 register = 0 (low-speed on-chip oscillator on)
4. Bits FRA22 to FRA20 in the FRA2 register:
   All division mode can be set when VCC = 2.7 V to 5.5 V 000b to 111b
   Divide ratio of 8 or more when VCC = 1.8 V to 5.5 V 110b to 111b (divide-by-8 or more)
5. When setting the FRA01 bit to 0 (low-speed on-chip oscillator selected), do not set the FRA00 bit to 0 (high-speed on-chip oscillator off) at the same time. Set the FRA00 bit to 0 after setting the FRA01 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRA0 register.

Figure 2.1 High-Speed On-Chip Oscillator Control Register 0 (FRA0) Setting

System Clock Control Register 3 (CM3)

Address	0009h							
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit(1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM35	CPU clock division when exiting wait mode select bit (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6	R/W
b7	CM37		0 0: MCU exits with the CPU clock immediately before entering wait or stop mode. 0 1: Do not set. 1 0: ~~High-speed on-chip oscillator clock selected~~ (3) → Do not set. 1 1: XIN clock selected (4)	R/W

1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register is set to 00b (no division mode).
3. ~~When bits CM37 and CM36 are set to 10b (high-speed on-chip oscillator clock selected), the following will be set when the MCU exits wait mode or stop mode.~~
4. OCD2 bit in OCD register = 1 (on-chip oscillator selected)
5. FRA00 bit in FRA0 register = 1 (high-speed on-chip oscillator on)
6. FRA01 bit in FRA0 register = 1 (high-speed on-chip oscillator selected)
7. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
8. OM05 bit in OM0 register = 1 (XIN clock oscillates)
9. OM13 bit in OM1 register = 1 (XIN-XOUT pin)
10. OCD2 bit in OCD register = 0 (XIN clock selected)
11. When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.
12. However, if an externally generated clock is used as the XIN clock, do not set bits CM37 to CM36 to 11b (XIN clock selected).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

Figure 2.2 System Clock Control Register 3 (CM3) Setting

Timer RC Control Register 1 (TRCCR1)

Address	0121h							
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4	R/W
b5	TCK1		0 0 0: f1	R/W
b6	TCK2		0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: ~~fOCO40M~~ 1 1 1: ~~fOCO-F~~ (2) → Do not set.	R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear TRC counter by input capture or by compare match in TRCGRA	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. ~~To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.~~

Figure 2.3 Timer RC Control Register 1 (TRCCR1) Setting

Timer RD Control Register i (TRDCRi) (i = 0 or 1)

Address	0140h (TRDCR0), 0150h (TRDCR1)							
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR2	CCLR1	CCLR0	CKEG1	CKEG0	TCK2	TCK1	TCK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0	R/W
b1	TCK1		0 0 0: f1	R/W
b2	TCK2		0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRDCLK input (1) or fC2 (2) 1 1 0: ~~fOCO40M~~ 1 1 1: ~~fOCO-F~~ (5) → Do not set	R/W
b3	CKEG0	External clock edge select bit (3)	b4 b3	R/W
b4	CKEG1		0 0: Count at the rising edge 0 1: Count at the falling edge 1 0: Count at both edges 1 1: Do not set.	R/W
b5	CCLR0	TRDi counter clear select bit	b7 b6 b5	R/W
b6	CCLR1		0 0 0: Disable clear (free-running operation)	R/W
b7	CCLR2		0 0 1: Clear by input capture in the TRDGRAi register 0 1 0: Clear by input capture in the TRDGRBi register 0 1 1: Synchronous clear (clear simultaneously with other timer RDi counter) (4) 1 0 0: Do not set. 1 0 1: Clear by input capture in the TRDGRCi register 1 1 0: Clear by input capture in the TRDGRDi register 1 1 1: Do not set.	R/W

Notes:
1. Enabled when the ITCLKi bit in the TRDECR register is set to 0 (TRDCLK input) and the STCLK bit in the TRDFCR register is 1 (external clock input enabled).
2. Enabled when the ITCLKi bit in the TRDECR register is set to 1 (fC2) in timer mode.
3. Enabled when bits TCK2 to TCK0 are set to 101b (TRDCLK input or fC2), the ITCLKi bit in the TRDECR is set to 0 (TRDCLK input), and the STCLK bit in the TRDFCR register is set to 1 (external clock input enabled).
4. This setting is enabled when the SYNC bit in the TRDMR register is set to 1 (registers TRD0 and TRD1 operate synchronously).
5. ~~To select fOCO-F, set it to the clock frequency higher than the CPU clock frequency.~~

Figure 2.4 Timer RD Control Register 0, 1 (TRDCR0, TRDCR1) Setting

A/D Mode Register (ADMOD)

Address	00D4h							
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	MD2	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Division select bit	b1 b0	R/W
b1	CKS1		0 0: fAD divided by 8 0 1: fAD divided by 4 1 0: fAD divided by 2 1 1: fAD divided by 1 (no division)	R/W
b2	CKS2	Clock source select bit (1)	0: Selects f1 1: ~~Selects fOCO-F~~ → Do not set.	R/W
b3	MD0	A/D operating mode select bit	b5 b4 b3	R/W
b4	MD1		0 0 0: One-shot mode	R/W
b5	MD2		0 0 1: Do not set. 0 1 0: Repeat mode 0 0 1 1: Repeat mode 1 1 0 0: Single sweep mode 1 0 1: Do not set. 1 1 0: Repeat sweep mode 1 1 1: Do not set.	R/W
b6	ADCAP0	A/D conversion trigger select bit	b7 b6	R/W
b7	ADCAP1		0 0: A/D conversion starts by software trigger (ADST bit in ADCON0 register) 0 1: A/D conversion starts by conversion trigger from timer RD 1 0: A/D conversion starts by conversion trigger from timer RC 1 1: A/D conversion starts by external trigger ($\overline{\text{ADTRG}}$)	R/W

Notes:
1. When the CKS2 bit is changed, wait for 3 ϕAD cycles or more before starting A/D conversion.

If the ADMOD register is rewritten during A/D conversion, the conversion result is undefined.

Figure 2.5 A/D Mode Register (ADMOD) Setting

2.2 Change in the Flash Memory Suspend Function

For the flash memory suspend function, a program cannot be operated while auto-erasure is being suspended [refer to Figure 2.6].

Executable Operation during Suspend

		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	×	×	×	×	⊖	○	—	—	—	×	⊖	○(5)
	Program ROM	—	—	—	×	⊖	○	×	×	×	×	⊖	○

Not executable (*)

Notes:

1. ○ indicates operation is enabled by using the suspend function, × indicates operation is disabled, and — indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The operation of block blank check is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.
5. The program ROM area can be read with the BGO function while programming or block erasing data flash.

* : Not executable when using a data flash driver.

Figure 2.6 Change in the Flash Memory Suspend Function

2.3 Change in the Flash Memory Suspend Function's Electrical Characteristics

Allow 33 ms or more of the suspend during flash memory auto-erasure [refer to Figure 2.7].

Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Interval from erase start/restart until following suspend request		~~0~~ → 33	–	–	~~µs~~ → ms
–	Suspend interval necessary for auto-erasure to complete		~~20~~ → 33	–	–	ms

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.

Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Interval from erase start/restart until following suspend request		~~0~~ → 33	–	–	~~µs~~ → ms
–	Suspend interval necessary for auto-erasure to complete		~~3~~ → 33	–	–	ms

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.

Figure 2.7 Electrical Characteristics of the Flash Memory Suspend Function

2.4 Note on XCIN Clock

The XIN-XOUT pin and XCIN-XCOUT pin are shared pins (P4_6 and P4_7) in the R8C/32A Group, R8C/33A Group, and R8C/3GA Group. The XCIN clock cannot be used when using the XIN clock.

3. Slated Changes

Contact the Renesas Technology sales department for products including the high-speed on-chip oscillator.