NEC

Customer Notification

QB-MINI2-EE

Universal Flash Memory Programmer and Serial On-chip Debugger

Operating Precautions

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(A) Table of Operating Precautions

No.	Target Device	Debug/ Progr.	Outline	Control Code: / Firmware:	QB-MINI2-EE A V4.00	A V4.01	A V4.02	A V4.03	A V4.04	A V4.05	A V4.07	A V5.00
1	78K0	Debug	Invalid internal high-speed RAM area after RESET		×	×	×	×	×	×	×	×
2	V850	Debug	Use of watchdog timer		×	×	×	×	×	×	×	×
3	V850	Debug	Break during sub-clock operation		×	×	×	×	✓	✓	✓	✓
4	V850	Debug	Break during flash memory modifications		×	×	×	×	×	×	×	×
5	V850	Debug	Reset vector handling		×	×	×	×	×	×	×	×
6	V850	Debug	Modifying specific registers		×	×	×	×	×	×	×	×
7	V850	Debug	Reset generation		×	×	×	×	×	×	×	×
8	78K0S	Debug	Debugging with operation clock of 6MHz or lower		✓	✓	✓	✓	✓	✓	✓	✓
9	78K0S	Debug	Downloading when operation clock is 10MHz		×	✓	✓	✓	✓	✓	✓	✓
10	78K0S	Debug	Display of register values		✓	✓	✓	✓	✓	✓	✓	✓
11	78K0R	Debug	Breakpoint for a CPU lower than 2MHz		×	×	✓	✓	✓	✓	✓	✓
12	78K0R	Debug	Debugging of time measurement function in 1-wire mode		×	×	✓	✓	✓	✓	✓	✓
13	78K0R	Debug	Invalid operation after program download		×	×	✓	✓	✓	✓	✓	✓
14	78K0R	Debug	Using QB-MINI2-EE with USB1.1		×	×	×	✓	✓	✓	✓	✓
15	78K0R	Debug	Operation at frequencies at 20MHz		×	×	×	✓	✓	✓	✓	✓
16	78K0R	Debug	General purpose registers after reset		×	×	×	×	×	×	×	×
17	78K0R	Debug	Specification changes in conjunction with firmware optimization		-	-	-	✓	✓	✓	✓	✓
18	78K0R	Debug	Hardware breakpoints		×	×	×	×	×	×	×	×
19	V850	Debug	Download speed via CSI		-	-	-	-	✓	✓	✓	✓
20	V850	Debug	Reserved area changed for CSI		-	-	-	-	✓	✓	✓	✓
21	V850	Debug	Operation in low voltage		-	-	-	-	×	×	×	×
22	78K0R	Debug	Addition of specification of RRM and DDM functions		-	-	-	-	-	✓	✓	✓
23	78K0	Debug Progr.	Devices with TOOLCx and TOOLDx pins		-	-	-	-	-	-	✓	✓
24	All	Debug Progr.	Addition of specification for support of MINICUBE2 wireless unit (QB-MINI2-RF)		-	-	-	-	-	-	-	✓

- : Not relevant or the target device is not supported
✓ : Not applicable or new/changed specification applies
× : Applicable

(B) Description of Operating Precautions

No.1	Invalid internal high-speed RAM area after RESET
	Details If a RESET signal is generated at the RESET-pin or a RESET occurs due to POC during program execution, below showed internal high-speed RAM areas become invalid: - 5 bytes from FECBh to FECFh (When ***Permit*** is selected in ***Target Power OFF*** field in the configuration dialog box) - 10 bytes from FEC9h to FECFh and FEDDh to FEDFh (When ***Not Permit*** is selected in ***Target Power OFF*** field in the configuration dialog box)
	Workaround No workaround available

No.2	Use of watchdog timer
	Details The watchdog timer cannot be used, because it's forcibly stopped by the debug monitor program. Don't set the option byte to disable watchdog timer stop.
	Workaround No workaround available

No.3	Break during sub-clock operation
	Details In the configuration dialog box of the debugger it's possible to define, if the operating clock during a break is switched from sub-clock to main clock. But if UART is the communication channel between QB-MINI2-EE and target device, an occurring break during sub-clock operation (while the main clock has been stopped) will forcibly switch the operation clock to main clock. The device continues its operation with the main clock after monitor program execution.
	Workaround No workaround available

No.4	Break during flash memory modifications
	Details A break may occurs at an unexpected address during flash memory modifications (for example usage of flash self-programming libraries).
	Workaround Reset the device and repeat program execution.

No.5	Reset vector handling
	Details The reset vector cannot be used.
	Workaround No workaround available

No6	Modifying specific registers
	Details Peripheral I/O registers (except PCC and CKC), that require a specific program sequence for access, cannot be modified in the I/O register of the debugger.
	Workaround No workaround available

No.7	Reset generation
	Details A break occurs, when an external reset (which isn't masked in the debugger GUI) or an internal reset is generated.
	Workaround No workaround available

No.8	Debugging with operation clock of 6MHz or lower
	Target Device 78K0S *Details* The debugger does not start when the target device operating frequency is 6MHz or lower
	Workaround No workaround available. This item is corrected from firmware version V4.00 onwards.

No.9	Downloading when operation clock is 10MHz
	Target Device 78K0S *Details* When the target device operating frequency is 10MHz, an error will occur during download of a program and the downloading cannot be completed.
	Workaround No workaround available

No.10	Display of register values
	Target Device 78K0S *Details* Register values may be displayed incorrectly in the debugger during a break.
	Workaround This item is corrected in firmware version V4.00

No.11	Breakpoint for a CPU lower than 2MHz

Target Device
78K0R

Details
If a break occurs, during CPU operational clock lower than 2MHz, the internal flash memory can no longer be rewritten. The following operations cannot be performed any longer.

1. Writing to internal Flash memory
2. Setting or canceling of software breakpoints
3. Starting execution at the set software breakpoint position
4. Step execution at the set software breakpoint position
5. Step-over execution, Return Out execution
6. Run to Cursor
7. If Permit of 'Flash memory access in the Flash Programming area', is selected in the Configuration dialog box, the following operations cannot be performed.

    a. Setting, changing, or canceling of hardware breaks
    b. Masking/unmasking of internal reset
    c. Switching of peripheral breaks

Workaround

To set a breakpoint, for operation performed at a CPU clock lower than 2MHz, use a hardware break and not a software breakpoint

No.12	Debugging of time measurement function in 1-wire mode

Target Device
78K0R

Details
When debugging is performed in 1-wire mode (selected by choosing TOOL0 in the Target Device Connection area in the configuration dialog box of the debugger), the Run-Break execution time is measured with the accuracy of about 10ms.

Workaround

Perform debugging in 2-wire mode (TOOL0 + TOOL1)

No.13	Invalid operation after program download

Target Device
78K0R

Details
When the reset vector (address 0 and 1) points to an address lower than 0x0100, the debugger operation becomes invalid after a program is downloaded. Specifically, illegal breaks occur immediately after execution, the source window cannot be opened, and the application cannot be debugged.

Workaround

Assign the reset vector for the user program to addresses of 0x0100 or higher.

No.14	Using QB-MINI2-EE with USB1.1
	Target Device 78K0R *Details* The debugger operation may become invalid if it is connected via USB 1.1.
	Workaround This item has been corrected in firmware V4.03.

No.15	Operation on frequencies •20MHz
	Target Device 78K0R *Details* When the QB-MINI2 operates at a frequency of 20 MHz or higher, downloading or manipulation to change the memory contents may fail.
	Workaround Perform downloading or manipulation to change the memory contents at a frequency lower than 20MHz. This item has been corrected in firmware V4.03.

No.16	General purpose registers after reset
	Target Device 78K0R *Details* After reset in standby mode, the general register contents are not retained.
	Workaround There is no workaround.

No.17	Specification changes in conjunction with firmware optimization

Target Device
78K0R

Details
The specifications shown below have been changed or added in conjunction with firmware optimization.

This item has been implemented in firmware V4.03. To apply this correction, use the NEC Electronics debugger ID78K0R-QB V3.30 or later.

1. The debugger operation speed has been improved by improving the MINICUBE2 firmware processing.
2. The operation speed in 1-wire mode has been improved to be equalized with that in 2-wire mode.
3. For a case when the pseudo real-time monitor function (RRM function) is not used during debugging in 2-wire mode, the occupied size of the debug monitor program allocated to the last block in the internal ROM has been reduced from 1 KB to 88 bytes.
4. Instructions that perform two instructions during step-wise execution have been modified so as to perform only one instruction.
5. The option byte setting (C1H) for the LVI default start function is now the same regardless of whether MINICUBE2 is connected.
6. Debugger operations for rewriting the flash memory (download, software break setting, etc.), which were not possible when the target microcontroller cannot rewrite the flash memory due to the CPU clock or the regulator mode, are now available by changing the specification so that the debugger automatically changes the SFR contents so as to enable rewriting of the flash memory to enable such operations. (Correction of restriction No. 11 is also included in this change). After rewriting the flash memory is completed, the SFR contents will be restored. The debugger will output the following errors if the operation voltage is lower than the voltage with which flash memory rewriting is possible (1), or if the flash memory rewriting is prohibited by the debugger configuration (2).
   (When using the ID78K0R-QB)
   In case of (1): “F0C37: The voltage is too low to operate flash programming.”
   In case of (2): “F0C48: Flash programming is disabled in the debugger.”
   In case of (1) or (2) and when setting or cancelling software breaks:
   “W401C: Software break can not be set on this area.”
7. A break, which was generated if STOP mode is entered when the pseudo RRM function is used, is now prevented by releasing the STOP mode.

Workaround

There is no workaround.

No.18	Hardware breakpoints
	Target Device 78K0R *Details* A hardware break occurs at an address several instructions after the specified point. This applies to both instruction fetch and data access. If any of the following debugger operations <1> to <3> is performed while the flash memory cannot be rewritten, a hardware break occurs at an address several instructions after the specified point. 1. Step-wise execution 2. Return Out execution 3. Come Here.
	Workaround There is no workaround.

No.19	Download speed via CSI
	Target Device V850 *Details* The downloading speed via the CSI interface with the target system has been approximately doubled. This specification change is applicable for firmware V4.04 or later. - Using the GHS Multi debugger, use the 850eserv V12.0 or later - Using the IAR debugger, use the IAR workbench V3.40 or later
	Workaround There is no workaround.

No.20	Reserved area changed for CSI
	Target Device V850ES/IE2 *Details* The reception error interrupt can now be used with Minicube2 when connected to the target system via CSI interface. The change has been implemented for the purpose of preventing debugger hang-up when a reception error occurs. This specification change is applicable for firmware V4.04 or later. - Using the GHS Multi debugger, use the 850eserv V12.0 or later - Using the IAR debugger, use the IAR workbench V3.40 or later When using the latest V850eserv and IAR version, it does not start with the firmware V4.03 or earlier. Also be sure to upgrade the firmware to V4.04 or later, if the V850eserv and IAR version 3.40 is used and Minicube2 is connected to the target system with UART.
	Workaround There is no workaround.

No.21	Operation at low voltage
	Target Device V850ES/JF3-L, V850ES/JG3-L *Details* When the operation voltage of less 2.7V, communication between Minicube2 and the target device cannot be performed correctly, and a malfunction occurs. Be sure to perform debugging at a voltage of at least 2,7V.
	Workaround There is no workaround.

No.22	Specification on RRM and DDM functions
	Target Device 78K0R *Details* The following specifications <1> to <3> have been added. These specifications are added to firmware V4.05 and later. <1> The pseudo RRM function is now supported in 1-wire mode (supported only in 2-wire mode in older version) <2> The entire memory space can now be monitored when using the pseudo RRM function. If the targets to be monitored are too numerous, the operability of the debugger may be affected because the monitoring speed is slow when using the pseudo RRM function in 1-wire mode. Therefore monitoring the by Watch window, rather than the memory window, is recommended. <3> The direct memory modification (DDM) function is now supported. Along with this support, the contents in the RAM can now be changed during program execution. When changing the memory contents by using the DDM function, program execution is stopped. This means, that the memory contents are not changed in real time.

No.23	Devices with TOOLCx and TOOLDx pins
	Target Device 78K0 *Details* On-chip debugging and flash programming of devices that have the TOOLCx and TOOLDx pins can now be executed. This specification is added in firmware V4.07 and later. If you are using the NEC Electronics debugger ID78K0-QB, please switch to ID78K0-QB V3.10 or later. *Caution* When the ID78K0-QB is upgraded to V3.10, be sure to upgrade the firmware of the MINICUBE2 to V4.07 or later.

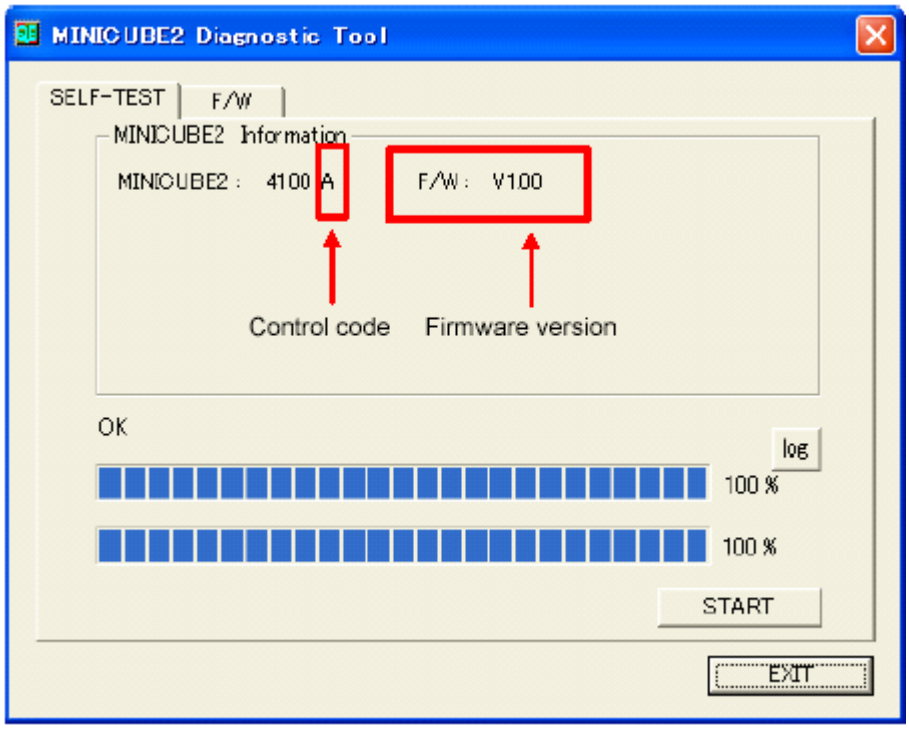
No.24	Addition of specification for support of MINICUBE2 wireless unit (QB-MINI2-RF)
	Target Device All *Details* The wireless extension unit QB-MINI2-RF for MINICUBE2 is now supported. This specification is added to firmware V5.00 or later. *Caution* This unit can be used for all 78K0S, 78K0, 78K0R, and V850 microcontrollers, but whether a microcontroller is supported varies depending on the version of the debugger used.

(C) Product Version

The **“Control Code”** is an alphabetic code used to identify the hardware of QB-MINI2-EE. It is the second digit from the left in the 10-digit serial number printed on the sticker attached to the bottom side of QB-MINI2-EE (if it has not been upgraded).

The **“Firmware”** (F/W) is a program embedded in the controller device of the QB-MINI2-EE. The F/W version is shown as Vx.xx.

The control code and firmware version can be checked with the QB-MINI2-EE diagnostic tool:



(D) Supported Devices

The devices that are supported by QB-MINI2 are listed in the following table:

1. 78K0 microcontrollers

   the following table lists the support status for 78K0 microcontrollers. Support for the target device also differs depending on the version of the development tools.

Supported Devices	On-chip Debugging						Flash Memory Programming			
	Firmware Version	ID78K0-QB Version	Device File Package		Debug Monitor Area Size		Firmware Version	QBP Version	Parameter File Package	
				Version	w/o RRM	w RRM				Version
78K0/Lx2	≥V1.00	≥V2.94	DF780397	≥V1.03	256 bytes	256 bytes	≥V1.00	≥V1.00	PRM78F0397	≥V1.02
78K0/Kx2	≥V1.00	≥V2.94	DF780547	≥V2.21	256 bytes	256 bytes	≥V1.00	≥V1.00	PRM78F0547	≥V1.07
78K0/Kx2-L	≥V4.07	≥V3.10	DF780588	≥V2.00	256 bytes	384 bytes	≥V4.07	≥V2.24	PRM78F0588	≥V1.01
78K0/Ix2	≥V4.07	≥V3.10	DF780756	≥V1.00	256 bytes	384 bytes	≥V4.07	≥V2.24	PRM78F0756	≥V1.00
78K0/Kx1+	≥V4.01	≥V2.94	DF78F0148H	≥V3.00	256 bytes	256 bytes	≥V1.00	≥V1.00	PRM78F0148	≥V1.12
UPD78(F)0822B	Not supported						≥V1.00	≥V1.00	PRM78F0822	≥V1.00
78K0/Fx2	≥V4.01	≥V2.94	DF78F0893	≥V1.01	384 bytes	512 bytes	≥V1.00	≥V1.00	PRM78F0893	≥V1.04
78K0/Fx1+	≥V4.01	≥V2.94	DF78F0876	≥V1.10	256 bytes	384 bytes	≥V1.00	≥V1.00	PRM78F0876	≥V1.11
UPD78F0822B	Not supported						≥V1.00	≥V1.00	PRM78F0822	≥V1.00
UPD78F0711 UPD78F0712 UPD78F0714	≥V4.01	≥V2.94	DF78F0714	≥V1.10	256 bytes	384 bytes	≥V1.00	≥V1.00	PRM78F0714	≥V1.12
UPD78F0730	≥V4.01	≥V2.94	DF780731	≥V1.20	256 bytes	256 bytes	≥V1.00	≥V1.00	PRM78F0731	≥V1.03
UPD78F0862x	Not supported						≥V1.00	≥V1.00	PRM78F0862	≥V1.11
UPD179F11x UPD179F12x	≥V4.04	≥V2.94	DF179124	≥V1.00	256 bytes	256 bytes	≥V4.03	≥V2.22	PRM179F124	≥V1.00
78K0/Lx3	≥V4.01	≥V2.94	DF780495	≥V1.00	256 bytes	256 bytes	≥V4.03	≥V2.21	PRM78F0495	≥V1.01
78K/Kxx with LIN	Not supported						≥V1.00	≥V1.00	PRM78F8006H	≥V1.00
							≥V1.00	≥V1.00	PRM78F8016	≥V1.01
							≥V1.00	≥V1.00	PRM78F8020	≥V1.01
UPD78F8024 UPD78F8025	Not supported						≥V1.00	≥V1.00	PRM78F8025	≥V1.00

2. 78K0S microcontrollers

the following table lists the support status for 78K0S microcontrollers. Support for the target device also differs depending on the version of the development tools. Check the external interrupt pins that can be used as a communication interface between Minicube2 and the target device.

Supported Devices	On-chip Debugging					Flash Memory Programming			
	Supported Serial Interface	Firmware Version	ID78K0-QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
78K0S/KU1+	INTP1	≥V4.01	≥V2.90	DF789234	≥V3.20	≥V3.00	≥V1.00	PRM78F9234	≥V1.08
78K0S/KY1+									
78K0S/KA1+	INTP3								
78K0S/KB1+									
UPD78F9334	Not supported					≥V3.00	≥V1.00	PRM78F9334	≥V1.00

3. 78K0R microcontrollers

the following table lists the support status for 78K0R microcontrollers. Support for the target device also differs depending on the version of the development tools.

Supported Devices	On-chip Debugging				Flash Memory Programming			
	Firmware Version	ID78K0-QB Version	Device File Package	Version	Firmware Version	QBP Version	Parameter File Package	Version
78K0R/Kx3	≥V4.03	≥V3.30	DF781188	≥V3.00	≥V4.00	≥V2.00	PRM-78F1188	≥V1.01
78K0R/KC3-L 78K0R/KD3-L 78K0R/KE3-L	≥V4.05	≥V3.50	DF781014	≥V2.00	≥V4.03	≥V2.24	PRM78F1014	≥V1.01
78K0R/KF3-L 78K0R/KG3-L	≥V5.00	≥V3.60	DF781014	≥V2.00	≥V4.03	≥V2.24	PRM78F1014	≥V1.01
78K0R/Ix3	≥V5.00	≥V3.60	DF781235	≥V2.00	≥V4.03	≥V2.24	PRM78F1235	≥V1.00
78K0R/Lx3	≥V5.00	≥V3.60	DF781508	≥V1.00	≥V4.03	≥V2.24	PRM78F1508	≥V1.00
78K0R/Fx3	≥V5.00	≥V3.60	DF781845	≥V1.00	≥V4.03	≥V2.24	PRM78F1845	≥V1.00
78K0R/Kx3-C	≥V5.00	≥V3.60	DF781849	≥V1.00	≥V4.03	≥V2.24	PRM78F1849	≥V1.00

4. V850 microcontrollers

the following table lists the support status for V850 microcontrollers. Support for the target device also differs depending on the version of the development tools. Check the serial interface that can be used as a communication interface between Mini2 and the target device.

Supported Devices	On-chip Debugging					Flash Memory Programming			
	Supported Interfaces	Firmware Version*	GHS eserv / IAR*	Device File Package	Version*	Firmware Version *	QBP Version*	Parameter File Package	Version*
V850ES/Hx2	UART0/CSIB0	V4.04	Vx.245/ V3.40	DF703712	V1.10	V2.00	V1.00	PRM70F3712	V1.00
V850ES/Hx3	UART0/CSIB0	V4.04	Vx.245/ V3.40	DF703757	V1.01	V4.04	V2.21	PRM70F3757	V1.00
V850ES/IE2	UART0/CSIB0	V4.04	Vx.245/ V3.40	DF703714	V1.00	V2.00	V1.00	PRM70F3714	V1.00
V850ES/Jx2	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703724	V1.00	V2.00	V1.00	PRM70F3724	V1.00
V850ES/Jx3	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703746	V1.00	V2.00	V1.00	PRM70F3746	V1.02
V850ES/Jx3-L	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703738	V1.10	V2.00	V1.00	PRM70F3738	V1.00
V850ES/Jx3-H	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703771	V1.00	V2.00	V1.00	PRM70F3771	V1.00
V850ES/Jx3-U	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703771	V1.00	V2.00	V1.00	PRM70F3771	V1.00
V850ES/Jx3-E	UART0 CSIF0/CSIF3	V5.00	Vx.245/ V3.60	DF703786	V1.00	Not supported			
V850ES/Kx2	UART0/CSIB0	V4.04	Vx.245/ V3.40	DF703734	V1.00	V2.00	V1.00	PRM70F3734	V1.01
V850ES/Kx1	Not supported					not supported			
V850ES/Kx1H	UART0 CSIB0	V4.04	Vx.245/ V3.40	DF703218	V2.01	V2.00	V1.00	PRM70F3218H	V1.11
V850ES/Kx1+	UART0 CSIB0	V4.04	Vx.245/ V3.40	DF703318	V1.01	V2.00	V1.00	PRM70F3318	V1.11
V850ES/Fx2	UARTA0/CSIB0	V4.04	Vx.245/ V3.40	DF703239	V2.13	V2.00	V1.00	PRM70F3239	V1.12
V850ES/Fx3	UARTD0/ CSIB0[Note1]	V4.04	Vx.245/ V3.40	DF703385	V1.20	V4.00	V2.00	PRM70F3385	V1.02
V850ES/Fx3-L	UARTD0/ CSIB0[Note1]	V4.04	Vx.245/ V3.40	DF703622	V1.00	V4.00	V2.00	PRM70F3622	V1.00
V850ES/Sx2	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703288	V2.11	V2.00	V1.00	PRM70F3288	V1.11
V850ES/Sx3	UART0 CSIB0/CSIB3	V4.04	Vx.245/ V3.40	DF703368	V1.01	V2.00	V1.00	PRM70F3368	V1.02
V850ES/SJ3-H V850ES/SK3-H	UART0 CSIB0/CSIB3	V5.00	Vx.245/ V3.60	DF703482	V1.00	V4.03	V2.24	PRM70F3482	V1.00
V850E/IA3 V850E/IA4	UARTA0/CSIB0	V4.04	Vx.245/ V3.40	DF703186	V3.00	V2.00	V1.00	PRM70F3184 PRM70F3186	V2.10
V850E/IF3 V850E/IG3	UARTA0/CSIB0	V4.04	Vx.245/ V3.40	DF703454	V1.00	V4.03	V2.21	PRM70F3454	V1.02
V850ES/IK1	UARTA0/CSIB0	V4.04	Vx.245/ V3.40	DF703329	V2.00	V2.00	V1.00	PRM70F3329	V1.20
V850ES/Dx2	Not supported					V2.00	V1.00	PRM70F3325	V1.10
V850ES/DG3 V850ES/DJ3	UARTA0/CSIB0	V5.00	Vx.245/ V3.60	DF703426	E2.00a	V2.01	not supported		
V850E/MA3	UARTA0/CSIB0	V4.04	Vx.245/ V3.40	DF703134	V2.00	V2.00	V1.00	PRM70F3134	V1.21
V850E/SV2	Not supported					V2.00	V1.00	PRM70F3166	V1.10
V850E/PG2	Not supported					V2.00	V1.00	PRM70F3414	V1.00
V850E/PHO3	Not supported					V4.03	V2.21	PRM70F3441	V1.00

[Note1] When using UARTD0, f_{RH} cannot be used as the CPU clock

* or higher version

(E) Valid Specification

Item	Date published	Document No.	Document Title
1	June 2006 or later	U17966E	QB-MINI2-EE Setup Manual
2	March 2008 or later	U18371E	QB-MINI2-EE User's Manual

(F) Revision History

Item	Date published	Document No.	Comment
1	June 2006	TPS-LE-OP-TMINI2-1	Release
2	August 2006	TPS-LE-OP-TMINI2-2	1st Update: 78K0S restrictions added
3	October 2006	TPS-LE-OP-TMINI2-3	2nd Update: 78K0R restrictions added
4	October 2006	TPS-LE-OP-TMINI2-4	3rd Update: Revision of items 11, 12 and 13
5	March 2007	U18674EE1V0IF00	4th Update: New Doc.-No. This document is a replacement of document TPS-LE-OP-TMINI2-4 Items 14 to 18 added Tables in Chapter (D) Supported Devices revised
6	April 2007	U18674EE2V0IF00	Items 19 and 20 added Tables in Chapter (D) supported devices revised
7	July 2008	U18674EE3V0IF00	Items 21 and 22 added Tables in Chapter (D) supported devices revised
8	May 2009	U18674EE4V0IF00	Item 23 added Tables in Chapter (D) supported devices revised
9	February 2010	U18674EE5V0IF00	Item 24 added Tables in Chapter (D) supported devices revised