NEC

Customer Notification

QB-780714

In-Circuit-Emulator

Operating Precautions

Target Device

uPD78(F)0714™ K0 Motor ASSP

Document No. EEDT-OP-0024-5.0
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(A) Table of Operating Precautions

No.	Outline		QB-780714			
		Ctrl.-Code	C	D	E	F
		Date	30.11.04	29.11.07	29.11.07	29.11.07
		I/O Version	V1.03 V2.03	V1.03 V2.03	V1.03 V2.03	V1.04 V2.04 V3.01
		FPGA Version	V2.20	V2.20	V3.01	V3.01
		CPU Evachip	0045	0051 1056	1064	1068
1	TM51 doesn't stop during peripheral break		Y	Y	Y	Y
2	Electrical port pin behaviour different to device		Y	Y	Y	Y
3	The noise filters of the ITENC input pins have no function		N	N	N	N
4	Clock source for ADC not correct		N	N	N	N
5	ADC cannot be triggered by TMW		N	N	N	N
6	Peripheral macros will operate during peripheral break when retry registers are accessed.		Y	N	N	N
7	TMH clock from TM50 maskable		N	N	N	N
8	WDT does not stop during HALT/STOP modes		N	N	N	N
9	RTO01/DCSEL01 output not correct		N	N	N	N
10	SFR write to ADC may fail if interrupts are used		N	N	N	N
11	Software break and interrupt request conflict		Y	N	N	N
12	Illegal software operation after software break		Y	N	N	N
13	Emulation of device version uPD78F0711 and uPD78F0712 not supported		Y	Y	N	N
14	LVI interrupt can be masked		Y	Y	N	N
15	SFR access to Port 2 or ADC may fail		Y	Y	Y	N

N : Not applicable

Y : Applicable

Note: The control code is the second letter from the left of the 10 digit serial number or in case of update the latest control code is mentioned on the version up sticker.

(B) Description of Operating Precautions

No. 1	TM51 doesn't stop during peripheral break
	Details When peripheral break is enabled and the internal On-chip oscillator is selected as clock source (TCL51 = 0x07), TM51 will not stop during break. *Workaround* None

No. 2	Electrical port pin behaviour different to device
	Details: The electrical characteristics of the port pins is different between device and tool, because of FPGA based implementation. Port 5 and TW0TO0..5 are different because they are implemented by discrete FET's. *Workaround:* None

No. 3	The noise filters of the ITENC input pins have no function
	Details: None *Workaround:* None

No. 4	Clock source for ADC not correct
	Details: The ADC is supplied by fx/4 instead of fx/1. *Workaround:* None

No. 5	ADC cannot be triggered by TMW
	Details: None *Workaround:* None

No. 6	Peripheral macros will operate during peripheral break when retry registers are accessed.
	Details: The peripheral clock will run for a few cycles when peripheral break is enabled and a SFR requiring “Retry” is accessed in break mode.Because of this, all peripheral macros will operate for these few additional cycles in that case (Access to SFR by SFR window, watch window or TCL console). *Workaround:* None

No. 7	TMH clock from TM50 maskable
	Details: When selecting TM50 as clock source for TMH0 (TMHMD0.CKS02..00 = 5), the clock input is masked if the output enable of TM50 is disabled (TMC50.TOE50 = 0). *Workaround:* Set TMC50.TOE50 = 1.

No. 8	WDT does not stop during HALT/STOP modes
	Details: When the mask option is set to “Internal On-chip oscillator can be stopped by software”, the WDT will not stop its operation when entering HALT or STOP mode. *Workaround:* Stop the WDT’s clock source (Main or internal On-chip oscillator) before entering HALT or STOP mode.

No. 9	RTO01/DCSEL01 output not correct
	Details: When enabling DCSEL01 (DCCTL01.DCEN01 = 1) while TimerW (TMW0) is active, the pins TW0TOn/RTP1n, n = 5..1, will not output the expected signals. *Workaround:* None

No. 10	SFR write to ADC may fail if interrupts are used
	Details: If an interrupt occurs while writing to an ADC SFR (any of ADM, ADS, PFM, PFT) the write data may become corrupted. *Workaround:* Disable interrupts before writing to any of these registers.

No. 11	Software break and interrupt request conflict
	Details: In case a software break occurs just before starting an interrupt routine, the following behaviour might happen: After return from break, the PC is located one byte before start address of interrupt routine, which results in not correct program execution. In the trace view the following instruction is displayed (which has no meaning): XCHW AX,AX *Workaround:* Use hardware break point

No. 12	Illegal software operation after software break
	Details: In case the byte following a software break has the value C0H, the value of PC, PSW and SP are not correct after return from break, which results in not correct program execution. *Workaround:* Use hardware break point

No. 13	Emulation of device version uPD78F0711 and uPD78F0712 not supported
	Details: None *Workaround:* None

No. 14	LVI interrupt can be masked
	Details: With the tool it's possible to mask the LVI interrupt using the MK0L.0 bit (LVIMK). Also it's possible to read or change the pending status of the interrupt using the IF0L.0 bit (LVIIF). This behaviour is different to the device. The device can neither mask the interrupt nor read or change the pending interrupt status. *Workaround:* Clear the MK0L.LVIMK bit and leave it cleared. Do not read or write the IF0L.LVIIF bit

No. 15	SFR access to Port 2 or ADC may fail
	Details: Access to any of the following SFR's may fail: P2, ADCR, ADM, ADS, PFM, PFT *Workaround:* None

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	September 2006	U17366	User's Manual
2	November 2007	EEDT-OP-0024-5.0	This document

(D) Revision History

Item	Date published	Document No.	Comment
1	September 2004	EEDT-OP-0024-1.0	1st release
2	October 2004	EEDT-OP-0024-2.0	2nd release
3	November 2004	EEDT-OP-0024-3.0	3rd release
4	July 2007	EEDT-OP-0024-4.0	4th release (Text correction)
5	November 2007	EEDT-OP-0024-5.0	5th release (Update to level “F”)