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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A047A/E	Rev.	1.00
Title	Precaution of using DTC(Data Transfer Controller)		Information Category	Technical Notification		
Applicable Product	Described below	Lot No. -	Reference Document	User's Manuals: Hardware of Applicable Products		

Several conditions are added to the following applied product in the User's Manual.

1. Applied Product

R8C/34E Group, R8C/34F Group, R8C/34G Group, R8C/34H Group

R8C/36E Group, R8C/36F Group, R8C/36G Group, R8C/36H Group

R8C/38E Group, R8C/38F Group, R8C/38G Group, R8C/38H Group

R8C/34W Group, R8C/34X Group, R8C/34Y Group, R8C/34Z Group

R8C/36W Group, R8C/36X Group, R8C/36Y Group, R8C/36Z Group

R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group

R8C/32G Group, R8C/32H Group, R8C/33G Group, R8C/33H Group

R8C/34P Group, R8C/34R Group

R8C/54E Group, R8C/54F Group, R8C/54G Group, R8C/54H Group

R8C/56E Group, R8C/56F Group, R8C/56G Group, R8C/56H Group

2. Regarding DTC precaution

2-1. Do not execute DTC transfer to interrupt control registers, while CPU is executing Read-Modify-Write command.

2-2. Change DTCENi0~DTCENi7 bits when the interrupt to these bits will not occur.

2-3. Do not execute DTC transfer to the address that CPU rewrites data by Read-Modify-Write command.

Item No.	Target address of Read-Modify-Write command	Applied address of DTC transfer
2-1	All address	Interrupt Control registers
2-2	DTC Activation Enable Register	Same DTC Activation Enable Register
2-3	Specified address	Same specified address

3. Detail explanation of DTC precaution

3-1. Do not execute DTC transfer to interrupt control registers, while CPU is executing Read-Modify-Write command.

As shown Figure 1. , the write operation to interrupt control register by DTC transfer is invalid, in case DTC transfer timing conflicts with timing of Read-Modify-Write execution to every address by CPU.

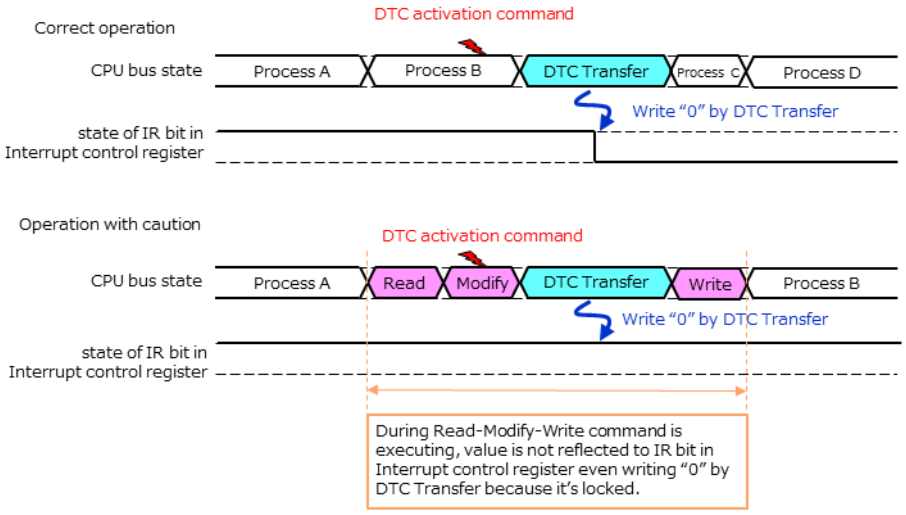

Figure 1. condition of CPU bus and interruptcontrol register

3-2. In case changing any of DTCENi0~DTCENi7 bit by Read-Modify–Write command, please change them when interrupt to these bits will not occur.

As shown Figure 2. , target bit to change to "0" will not occur, in case change timing from "1" to "0" of target bit in DTC Activation Enable Register(DTCENi) conflicts with timing of changing different bit in same register by Read-Modify-Write command by CPU.

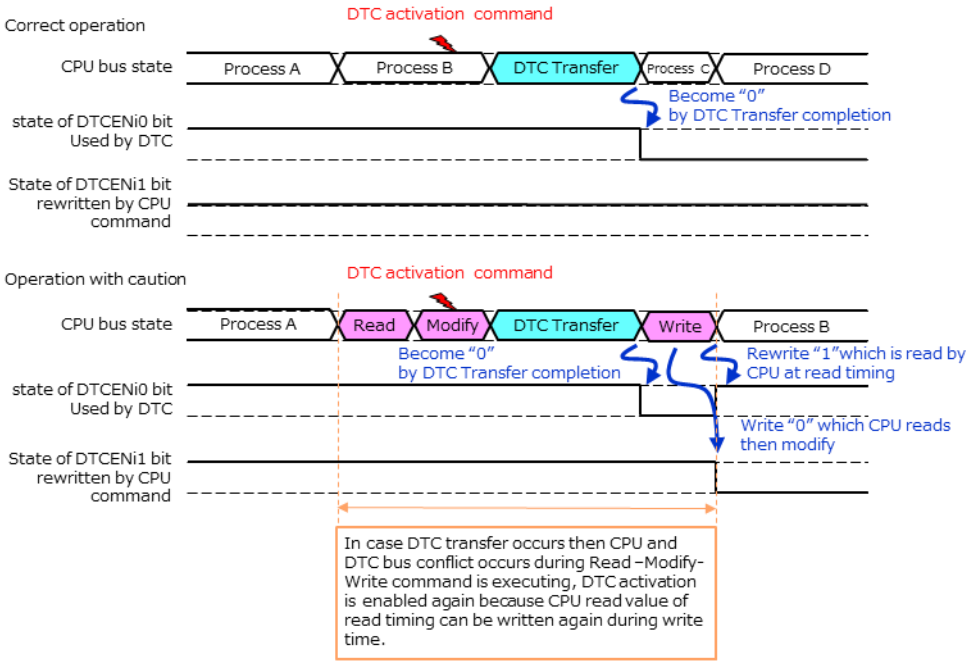

Figure 2. condition of CPU bus and DTC Activation Enable Register

3-3. Do not execute DTC transfer to the address that CPU rewrites data by Read-Modify-Write command.

As shown Figure 3. , write operation by DTC transfer may be invalid, in case rewrite to specific address by Read-Modify-Write command by CPU conflicts with write operation by DTC transfer.

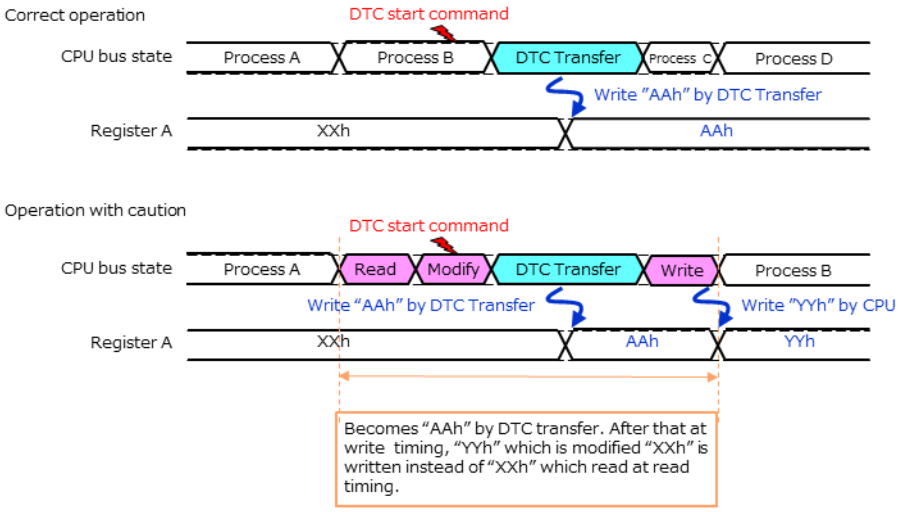

Figure 3. Condition of CPU bus and specific register

4. Regarding Read-Modify-Write command

R8C CPU designed to arbitrate bus not based on command but the bus access base. Bus access of Read-Modify-Write command execute as the following sequence and if DTC access trigger occurs during Read-Modify-Write command, the bus control is transferred from CPU to DTC after (1),(2).

The sequence of Read-Modify-Write command. The detail is refer to Figure 4.

1. Read the data at the specified address
2. Modify specified bit of the read data
3. Write the data to the original address

Data read and write are executed with byte or word access. In case BIT processing or logical calculation, unspecified data on the read data with byte or word access will be written to original address without any modification.

List of Read-Modify-Write command is shown in Table 1.

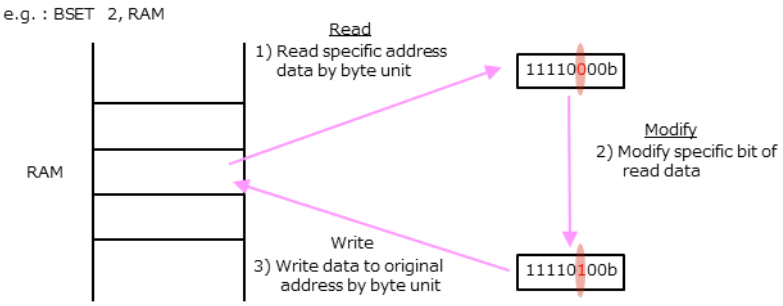

Figure 4. operation of Read-Modify-Write command

Table 1. List of Read-Modify-Write command

Function	Mnemonic
Transfer	MOVDir
Bit operation	BCLR, BMCnd, BNOT, BSET, BTSTC, BTSTS
Shift	ROLC, RORC, ROT, SHA, SHL
Calculation	ABS, ADC, ADCF, ADD, DADC, DADD, DEC, DIV, DIVU, DIVX, DSBB, DSUB, EXTS, INC, MUL, MULU, NEG, SBB, SUB
Logical calculation	AND,NOT,OR,XOR
Jump	ADJNZ,SBJNZ