RENESAS TECHNICAL UPDATE

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Title Precaution of using DTC(Data Transfer Using) Information Category Technical Notification Applicable Product Described below Image Information Image Information Image Information Category Technical Notification Several conditions are added to the following applied product in the User's Manuals: Hardware of Applicable Described below Reference Document User's Manuals: Hardware of Applicable Products 1. Applied Product R8C/34E Group, R8C/34F Group, R8C/34G Group, R8C/34B Group R8C/34E Group, R8C/34F Group, R8C/34G Group, R8C/34B Group R8C/34W Group, R8C/34S Group, R8C/34G Group, R8C/34G Group R8C/34W Group, R8C/34G Group, R8C/34G Group, R8C/34G Group R8C/34W Group, R8C/34G Group, R8C/34G Group, R8C/34G Group R8C/34B Group, R8C/34G Group, R8C/34G Group, R8C/34B Group R8C/34B Group, R8C/34G Group, R8C/34G Group, R8C/34G Group, R8C/34G Group R8C/34B Group, R8C/34G Group R8C/34B Group, R8C/34G Group R8C/34B Group, R8C/34G Gro	Product Category	MPU/MCU			Document No.	TN-R8C-A047A/E	Rev.	1.00			
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3. Detail explanation of DTC precaution

3-1. Do not execute DTC transfer to interrupt control registers, while CPU is executing Read-Modify-Write command.

As shown Figure 1., the write operation to interrupt control register by DTC transfer is invalid, in case DTC transfer timing conflicts with timing of Read-Modify-Write execution to every address by CPU.



Figure 1. condition of CPU bus and interrupt control register

3-2. In case changing any of DTCENi0~DTCENi7 bit by Read-Modify–Write command, please change them when interrupt to these bits will not occur.

As shown Figure 2., target bit to change to "0" will not occur, in case change timing from "1" to "0" of target bit in DTC Activation Enable Register(DTCENi) conflicts with timing of changing different bit in same register by Read-Modify-Write command by CPU.

CPU bus state	Process A	Yerocess B X DTC Transfer Xerocess cX Process D Become "0"
state of DTCENi0 bit Used by DTC		by DTC Transfer completion
State of DTCENi1 bit rewritten by CPU command		
Operation with caution		DTC activation command
CPU bus state	Process A	Read Modify DTC Transfer Write Process B
state of DTCENi0 bit Used by DTC		Become "0" by DTC Transfer completion Write "0" which CPU reads then modify
rewritten by CPU command		•
		In case DTC transfer occurs then CPU and DTC bus conflict occurs during Read -Modify- Write command is executing, DTC activation is enabled again because CPU read value of read timing can be written again during write time.



3-3. Do not execute DTC transfer to the address that CPU rewrites data by Read-Modify-Write command.

As shown Figure 3., write operation by DTC transfer may be invalid, in case rewrite to specific address by Read-Modify-Write command by CPU conflicts with write operation by DTC transfer.



Figure 3. Condition of CPU bus and specific register

4. Regarding Read-Modify-Write command

R8C CPU designed to arbitrate bus not based on command but the bus access base. Bus access of Read-Modify-Write command execute as the following sequence and if DTC access trigger occurs during Read-Modify-Write command, the bus control is transferred from CPU to DTC after (1),(2).

The sequence of Read-Modify-Write command. The detail is refer to Figure 4.

- 1. Read the data at the specified address
- 2. Modify specified bit of the read data
- 3. Write the data to the original address

Data read and write are executed with byte or word access. In case BIT processing or logical calculation, unspecified data on the read data with byte or word access will be written to original address without any modification.

List of Read-Modify-Write command is shown in Table 1.



Figure 4. operation of Read-Modify-Write command



Table 1. List of Read-Modify-Write command

Function	Mnemonic
Transfer	MOVDir
Bit operation	BCLR, BMCnd, BNOT, BSET, BTSTC, BTSTS
Shift	ROLC, RORC, ROT, SHA, SHL
Calculation	ABS, ADC, ADCF, ADD, DADC, DADD, DEC, DIV, DIVU, DIVX, DSBB, DSUB, EXTS, INC, MUL, MULU, NEG, SBB, SUB
Logical calculation	AND,NOT,OR,XOR
Jump	ADJNZ,SBJNZ

