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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0101A/E	Rev.	1.00
Title	Precaution of TPIU register access without connection of OCD emulator		Information Category	Technical Notification		
Applicable Product	RA6M4 Group, RA6M5 Group, RA6E1 Group, RA6T2 Group, RA4M2 Group, RA4M3 Group, RA4E1 Group	Lot No. All	Reference Document	Refer table at the end of this document		

Precaution of TPIU register access without connection of OCD emulator is added as follows.

Before modification

Table 2.8 Peripheral address map (for RA6M4, RA6M5, RA6E1, RA6T2, RA4M2, RA4M3)

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.14. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.14. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.14. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.14. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.14. References
TPIU	0xE004_0000	0xE004_0FFF	See reference 3. in section 2.14. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.14. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.14. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.14. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.9. CoreSight ATB Funnel and reference 4. in section 2.14. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.14. References
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.11. CoreSight Time Stamp Generator and reference 4. in section 2.14. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.14. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.14. References

After modification

Table 2.8 Peripheral address map (for RA6M4, RA6M5, RA6E1, RA6T2, RA4M2, RA4M3)

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.14. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.14. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.14. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.14. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.14. References
TPIU*1	0xE004_0000	0xE004_0FFF	See reference 3. in section 2.14. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.14. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.14. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.14. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.9. CoreSight ATB Funnel and reference 4. in section 2.14. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.14. References
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.11. CoreSight Time Stamp Generator and reference 4. in section 2.14. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.14. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.14. References

*1 : TPIU registers should not be accessed without connection of OCD emulator to avoid stopping bus access.

Before modification

Table 2.7 Peripheral address map (for RA4E1)

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.13. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.13. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.13. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.13. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.13. References
TPIU	0xE004_0000	0xE004_0FFF	See reference 3. in section 2.13. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.13. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.13. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.13. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.8. CoreSight ATB Funnel and reference 4. in section 2.13. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.13. References
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.10. CoreSight Time Stamp Generator and reference 4. in section 2.13. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.13. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.13. References

After modification

Table 2.7 Peripheral address map (for RA4E1)

Component name	Start address	End address	Note
ITM	0xE000_0000	0xE000_0FFF	See reference 2. in section 2.13. References
DWT	0xE000_1000	0xE000_1FFF	See reference 2. in section 2.13. References
BPU	0xE000_2000	0xE000_2FFF	See reference 2. in section 2.13. References
Secure SCS/SCS	0xE000_E000	0xE000_EFFF	See reference 1. in section 2.13. References
Non-Secure SCS	0xE002_E000	0xE002_EFFF	See reference 2. in section 2.13. References
TPIU*1	0xE004_0000	0xE004_0FFF	See reference 3. in section 2.13. References
ETM	0xE004_1000	0xE004_1FFF	See reference 1. in section 2.13. References
CTI1	0xE004_2000	0xE004_2FFF	See reference 2. in section 2.13. References
CTI0	0xE004_4000	0xE004_4FFF	See reference 4. in section 2.13. References
ATB Funnel	0xE004_7000	0xE004_7FFF	See section 2.8. CoreSight ATB Funnel and reference 4. in section 2.13. References
ETB	0xE004_8000	0xE004_8FFF	See reference 4. in section 2.13. References
Time Stamp Generator	0xE004_9000	0xE004_9FFF	See section 2.10. CoreSight Time Stamp Generator and reference 4. in section 2.13. References
System ROM Table	0xE00F_E000	0xE00F_EFFF	See reference 3. in section 2.13. References
Processor ROM Table	0xE00F_F000	0xE00F_FFFF	See reference 2. in section 2.13. References

*1 : TPIU registers should not be accessed without connection of OCD emulator to avoid stopping bus access.

Reference Document Table

Product	Document name
RA6M4 Group	Renesas RA6M4 Group User's Manual: Hardware Rev.1.30
RA6M5 Group	Renesas RA6M5 Group User's Manual: Hardware Rev.1.30
RA6E1 Group	Renesas RA6E1 Group User's Manual: Hardware Rev.1.10
RA6T2 Group	Renesas RA6T2 Group User's Manual: Hardware Rev.1.30
RA4M2 Group	Renesas RA4M2 Group User's Manual: Hardware Rev.1.30
RA4M3 Group	Renesas RA4M3 Group User's Manual: Hardware Rev.1.40
RA4E1 Group	Renesas RA4E1 Group User's Manual: Hardware Rev.1.10