Date: Jul. 4, 2023

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SY*-A0074B/E	Rev.	2.00
Title	Precaution regarding interrupt during successive bus access to peripherals sharing the same slave interfaces		Information Category	Technical Notification		
Applicable Product	S3A7 Group, S3S6 Group, S3A3 Group, S3A1 Group, S5D9 Group, S5D5 Group, S5D3 Group	Lot No. All	Reference Document	Refer table at the end of this document		

If all the conditions described below applies to your software, one of the following workarounds could be used to resolve observed unexpected software behavior:

[Condition]
All of the following conditions must be met:

a) Clock frequency setting:
   ICLK > PCLKx (x=A,B) (S3A1, S3A3, S3A6, S3A7)
   ICLK > PCLKx (x=A,B), ICLK>FCLK (S5D3, S5D5, S5D9)
b) A preceding access to the Slave interface or External bus (referred to as Access1) is followed by a subsequent access to the same slave interface or external bus (referred to as Access2).
c) No access to other Slave interfaces and External bus between Access1 and Access2 occurs.
d) An interrupt occurs on the last PCLKx/FCLK cycle of Access1.

Applicable slave interfaces and external bus:

Bus specifications (User's Manual: Hardware)
Table 15.1 for S5D3, S5D5, S5D9, S3A1, S3A6, and S3A7
Table 14.1 for S3A3

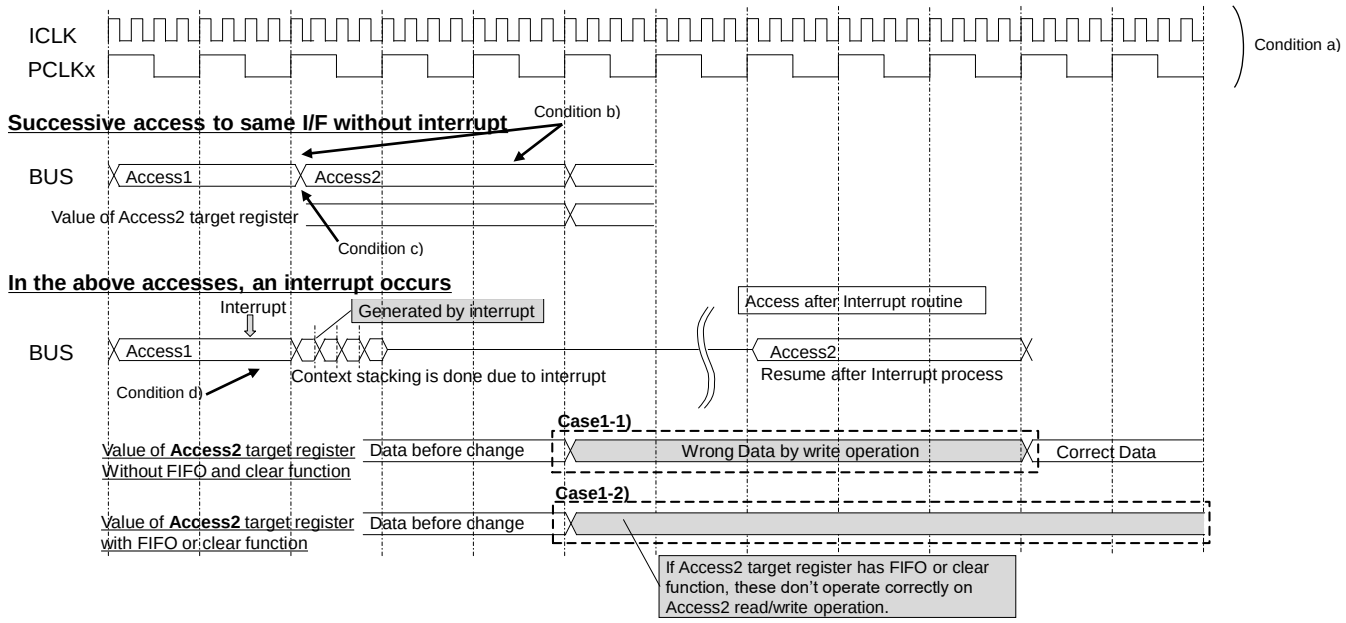
		S5D3	S5D5	S5D9	S3A1	S3A3	S3A6	S3A7
Slave interface	Memory bus 1	-	-	-	-	-	-	-
	Memory bus 2	-	-	-				
	Memory bus 3	-	-	-	-	-	-	-
	Memory bus 4	-	-	-	-	-	-	-
	Memory bus 5	-	-	-	-			-
	Internal peripheral bus 1	-	-	-	-	-	-	-
	Internal peripheral bus 3	✔	✔	✔	✔	✔	✔	✔
	Internal peripheral bus 4	✔	✔	✔	✔	✔	✔	✔
	Internal peripheral bus 5	✔	✔	✔	✔	✔	✔	✔
	Internal peripheral bus 7	✔	✔	✔	✔	✔	✔	✔
	Internal peripheral bus 8			✔				
	Internal peripheral bus 9	✔	✔	✔	-	-	-	-
External bus	CS area	-	-	-	-	-		-
	SDRAM area		-	-				
	QSPI area	✔	✔	✔	✔	✔		✔

[Precaution]
Case1 : A wrong access to Access2 target register might occur when all issue conditions meet.
1) When Access2 is write operation, wrong data is written to Access2 target register temporary, then a correct value is written after the CPU returning from interrupt.
2) If Access2 target register has FIFO or flag bit clear function, it causes unintentional value write to FIFO or unnecessary read from FIFO, or unintentional flag bit clear on the register.

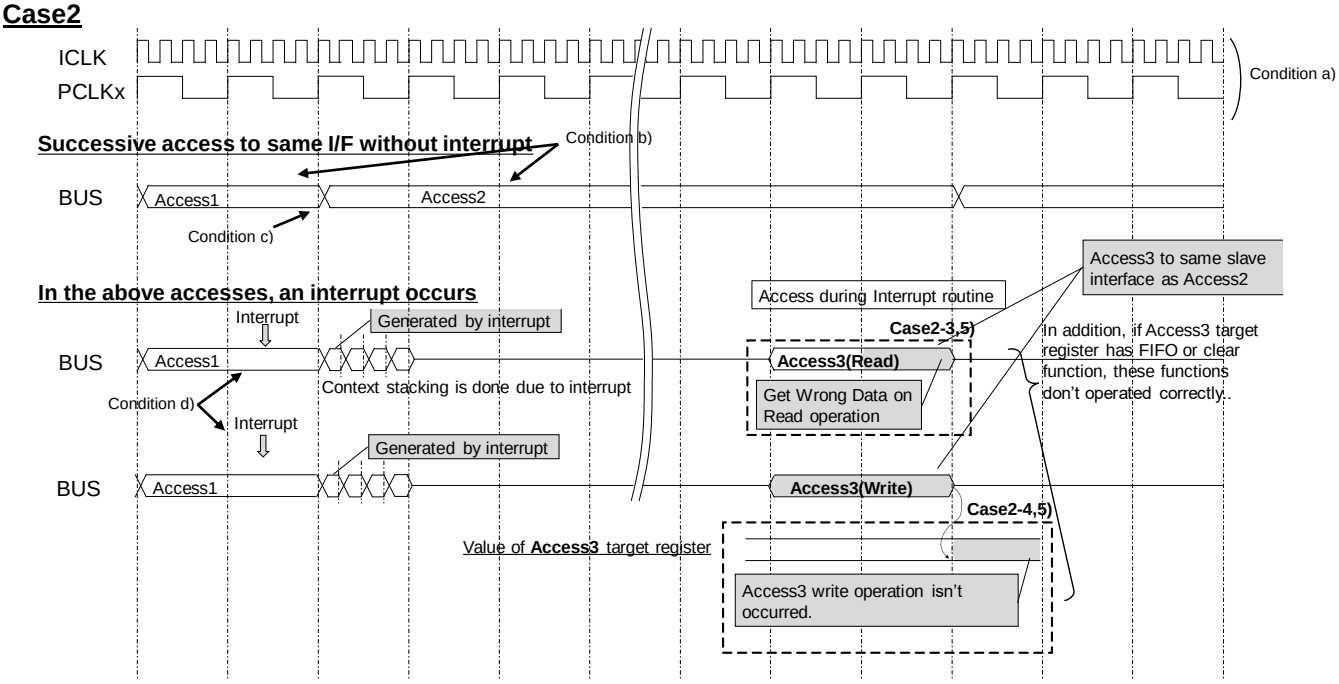
Case2 : A wrong access might occur in interrupt service routines when all issue conditions meet.
A register access to the same slave interface or external bus as Access2 in an interrupt service routine (referred to as Access3) causes an illegal operation
3) When Access3 is read operation, CPU might receive wrong data.
4) When Access3 is write operation, Access3 might not occurred in target register.
5) If Access3 target register has FIFO or flag bit clear function, these functions don't operated correctly.

*These behaviors may occur in combination.

Case1



Case2



[Workaround]
Apply one of the following workarounds.

1) In your system, set clock frequency as follows
   ICLK = PCLKx (x=A,B) (S3A1, S3A3, S3A6, S3A7)
   ICLK = PCLKx (x=A,B), ICLK>FCLK (S5D3, S5D5, S5D9)
2) Identify in your code where successive Access1 and Access2 occurs relevant to the area where the unintended SW behavior was observed. Then insert DSB instruction between Access1 and Access2
3) Disable Interrupts during Access1 to Access2

Note: Either one of the workarounds above will address the issue; therefore, choosing which one to apply will depend on your system requirements and behavior.

[Reference Documents]

Product Group	Document Name	Revision
S5D3	S5D3 Microcontroller Group User's Manual	Rev.1.10
S5D5	S5D5 Microcontroller Group User's Manual	Rev.1.30
S5D9	S5D9 Microcontroller Group User's Manual	Rev.1.30
S3A1	S3A1 Microcontroller Group User's Manual	Rev.1.20
S3A3	S3A3 Microcontroller Group User's Manual	Rev.1.10
S3A6	S3A6 Microcontroller Group User's Manual	Rev.1.20
S3A7	S3A7 Microcontroller Group User's Manual	Rev.1.40