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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A046A/E	Rev.	1.00
Title	Point for Caution Regarding Setting of the LCCR Register of the General PWM Timer (GPT)		Information Category	Technical Notification		
Applicable Product	RX62T Group, RX62G Group	Lot No. All lots	Reference Document	RX62T Group User's Manual: Hardware RX62G Group User's Manual: Hardware		

Thank you for your valued patronage and best wishes for your continued success in business.

This update is notification of a point for caution regarding operations when setting the LPSC[1:0] bits in the LCCR register of the general PWM timer (GPT).

1.1 Point for Caution

When setting the LPSC[1:0] bits in the LCCR register of the general PWM timer (GPT), observe the constraints below.

The frequency divisor of the LOCO dividing clock, selected by the LCCR.LPSC[1:0] bits, and that of IWDTCLK, selected by the CKS[3:0] bits in the IWDTCR register of the independent watchdog timer register (IWDT), should be in the following relation.

Frequency divisor selected by the LCCR.LPSC.LPSC[1:0] bits ≤ frequency divisor selected by the IWDTCR.CKS[3:0] bits

If the frequency divisor of the LOCO dividing clock is less than that of IWDTCLK, the counting of cycles of the frequency-divided clock derived from the LOCO will not proceed normally.

1.2 Action from Here

We will reflect this point in the hardware manuals for the RX62T and RX62G the next time they are revised.