NEC

Customer Notification

VR4181™

64-/32-Bit Microprocessor

Operating Precautions

μPD30181GM-66-8ED

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(A) Table of Operating Precautions

No.	Outline		μPD7030181GM-66-8ED			
		Rev.	V1.3			
		Rank[Note]	E			
1	MAIUINTREG access		✗			
2	Execution of hibernate / suspend sequence		✗			
3	Mode register setting for 64 Mbits SDRAM		✗			
4	MEMWR signal behavior at SDRAM access		✗			
5	The behavior after RTCRST		✗			
6	Usage of 64 MBit SDRAM I/F (5)		✗			
7	CBR Refresh interval		✗			
8	Burst CBR Refresh before/after self-refresh		✗			
9	Execution of wake-up sequence		✗			
10	USB client function		✗			
11	SDRAM burst refresh before Self-refresh		✗			
12	DRAM interface in SUSPEND mode		✗			
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15	Interrupt for DMA transfer		✗			
16	HAL timer operation		✗			
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19	CSI - Receive data		✗			
20	CSI - Send data		✗			
21	Usage of mflo/mfhi instruction within branch delay slot		✗			

✓ : Not applicable
✗ : Applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	MAIUINTREG access (Direction for use)
	Details When CPU read the MAIUINTREG (0x0B000090) in case of MISEN bit is set, it reads the contents of MIDATREG. This happens only when CPU reads the MAIUINTREG, in other words, CPU writes correct data into the MAIUINTREG. When you write the MAIUINTREG, write same value into work-memory (MISCREG in GIU, DRAM, etc) and refer to work-memory instead of the MAIUINTREG, if the contents of MAIUINTREG are needed.

No. 2	Execution of hibernate / suspend sequence (Direction for use)
	Details When CBR refresh is required, the memory controller unit waits for the external bus idle, and then holds the bus until CBR refresh is done. But when the memory controller unit is in self-refresh state, CBR refresh will not be executed. If CBR refresh is required while the memory controller unit is in self-refresh state, it will continue holding the external bus. Therefore CPU can not get any hibernate / suspend instruction codes from the ROM and VR4181 freeze during hibernate / suspend sequence. Put all hibernate / suspend instruction codes into the cache before executing hibernate / suspend sequence. The internal LCD controller and DMA controller must be stopped before executing hibernate / suspend sequence in order to avoid a DRAM access.

No. 3	Mode register setting for 64 Mbits SDRAM (Specification change notice)
	Details During the 64 Mbits SDRAM mode register write, A13 of the address bus is forced to logic "1". It should be set logic "0". During the 16 Mbits SDRAM mode register write, A13 had forced to logic "0". Use following sequence to initialize 64 SDRAM: (1) Set B0Config and B1Config bits of MEMCFG_REG(0x0A000304) register to "01" (2) Initialize SDRAM by setting Init bit of MEMCFG_REG to "1" (3) Set B0Config and B1Config bits to "10" before using SDRAM.

No. 4	MEMWR signal behavior at SDRAM access (Direction for use)
	Details The #MEMWR signal is active just before SDCLK is available when using SDRAM. For using a system, which has an external address decoder for an ISA device, apply follows: 1) Use VR4181 PCS [1:0] as chip select signal for external device and use LCDCS as chip select signal for external LCD controller. 2) Mask #MEMWR signal with #SYSEN signal and enable SYSDIR/#SYSEN function if PCS [1:0] are used as GPIO signal.

No. 5	The behavior after RTCRST (Direction for use)
	Details The #RTCRST initialization is one of the wake-up events. We recommend that hardware initial setting of clock div-mode, bus clock frequency, memory parameter, etc are done in full-speed mode just after RTCRST before going into hibernate-mode. Especially SDRAM initialize should be done just after RTCRST because SDRAM is in unknown state before initialize and its initialize can only be done by software.

No. 6	Usage of 64 MBit SDRAM I/F (5) (Documentation Errata)
	Details To prevent a possible deadlock, when the CPU requests cache line fill from 64 MBits SDRAM, do not set the TRP Bits in register SDTIMINGREG (0x0A00030C) to "00" or "01". Set TRP to "10" in register SDTIMINGREG, when 64 Mbits SDRAM is used.

No. 7	CBR Refresh interval (Specification change notice)

Details

Interval of CBR refresh after wake-up or resetSW reset is longer as expected.

Refresh timing is generated from detecting match between values of the internal up counter and BCURFCNTREG register. Therefore, when the BCURFCNTREG register value is changed to smaller than current value, and if the internal counter value is bigger than the new BCURFCNTREG register value, the next CBR refresh timing is at next match after the counter rounds over. After wake-up or resetSW reset, BCURFCNTREG is set to default (0x1FFF) and refresh counter starts counting. If this value will be changed by software, in most cases the counter has already passed this value and the interval is longer as expected. Insert short interval CBR refresh to cancel long CBR refresh interval after exiting self-refresh.

(1) Fill into cache (2), (3), (4), (5) and jump to cached routine.
(2) Set BCURFCNTREG to short interval (We recommend 250ns interval)
(3) Wait for execution of suitable number of CBR refresh by CP0 counter or RTC. In order not to prevent short interval CBR refresh, any external bus cycles should not appear.
(4) Set BCURFCNTREG to standard value.
(5) Return to main program.

No. 8	Burst CBR Refresh before/after self-refresh (Direction for use)

Details

When EDO interface is selected and BstRefr bit of MEMCFG_REG (0x0A000304) is set to 1 (enable burst refresh), the CPU applies a burst CBR refresh cycle just before and after self-refresh. When the CPU usually does distributive CBR refresh cycle, mixed use of burst and distributive CBR refresh occurs. This may not fit some DRAM specification.

Disable burst refreshes by reset BstRefr to 0 if DRAM prohibits mixed use of different refresh type. Moreover, if DRAM needs extra refresh cycle before/after self-refresh, insert short distributive CBR refresh interval.

No. 9	Execution of wake-up sequence (Direction for use)

Details

When SUSPEND bit of DRAMHIBCTL is set to 1 during wake-up, DRAM controller enters self-refresh state. When DRAM controller is in self-refresh state and CBR refresh request occurs, all next external bus cycles will not appear. Please refer for detail item (2) "Execution of hibernate / suspend sequence".

Exit from self-refresh state before CBR refresh request. Since BCURFCNTREG is reset to default value 0x1FFF, DRAM interface must be exited from self-refresh state within 0x1FFF Tclock (If (7) applies "CBR Refresh interval", 0x1FFF becomes more than 0x3FFF Tclock) Period from cold_reset.

No. 10	USB client function (Specification change notice)
	Details The VR4181's USB module is removed from specification

No. 11	SDRAM burst refresh before Self-refresh (Direction for use)
	Details If burst refresh is enabled by the BstRefr bit in MEMCFG_REG and the SUSPEND bit of DRAMHIBCTL register is set to 1, VR4181 applies a self-refresh command to SDRAM before burst CBR refresh. Therefore, SDRAM will exit from self-refresh mode. Disable burst refreshes by reset BstRefr. If SDRAM needs an extra refresh cycle before/after self-refresh, insert a short distributive CBR refresh interval.

No. 12	DRAM interface in SUSPEND mode (Direction for use)
	Details Do not apply SUSPEND instruction, when the DRMEN and STOP_CLK bits in DRAMHIBCTL register are set. To get into suspend mode proceed as follows: • clear STOP_CLK bit of the DRAMHIBCTL register • wait 1 us • clear the SUSPEND bit of the DRAMHIBCTL register • execute suspend instruction

No. 13	Internal clock in HIBERNATE mode (Direction for use)
	Details Internal clocks (Pclock, Tclock, etc) are running in Hibernate mode as long as Vdd2 power is supplied. To avoid an increase in the power consumption of the Hibernate current, cut Vdd2 power supply off in Hibernate mode by the MPOWER signal.

No. 14	Audio -in DMA transfer (Direction for use)
	Details To prevent a possible incorrect audio-in DMA transfer, don't use Tclock/8 (reset default) in ISA-BRGCTL (0x0B00 02C0) register. Set PCLK divisor rate to 1/1, 1/2, or 1/4 Tclock when Audio-in DMA transfer is executed.

No. 15	Interrupt for DMA transfer (Documentation Errata)
	Details Following description regarding interrupt during DMA transfer is correct: (1) Interrupt pending bits in DMAITRQREG (0x0A00 0662) can be cleared by writing '1' to the correspond bits. (2) When DMA transfer is set to auto-stop mode, secondary page of DMA buffer is not used in the DMA transfer (only primary page is used). (3) Vr4181 does not use the SSTOPEN bit in SCNTREG (0x0B00 0168). (4) Vr4181 does not use the MSTOPEN bit MCNTREG (0x0B00 0172).

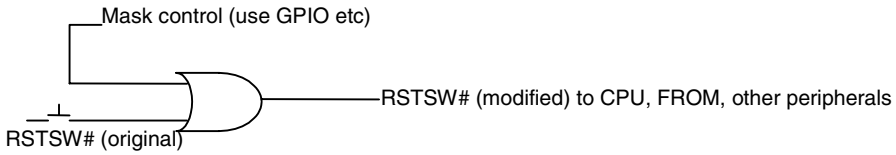
No. 16	Usage of HAL timer operation (Direction for use)
	Details For using the HAL timer shutdown make sure that: (a) TIMOUTRST bit in PMUINTREG (0x0B00-00A0) should be cleared as soon as possible after CPU has booted. Note: to clear this bit, write "1" to this bit (b) DRAM_EN, SUSPEND, STOP_CLK bit in DRAMHIBCTL (0x0B00-00B0) should be cleared before/during DRAM interface initialization.

No. 17	RSTSW# recognition during wake-up sequence (Direction for use)

Details

Vr4181 does not recognize RSTSW# signal until HAL timer is cleared during wake-up sequence. The PMU controls mask of RSTSW# reset for CPU core and internal peripherals. During Vr4181 waking-up sequence, PMU masks this reset until HAL timer is cleared (stopped) by software. If RSTSW# is activated during resume sequence from hibernate, Vr4181 will run normally until HAL timer clear although RSTSW# is active. If RSTSW# signal is also used for external peripheral reset, a conflict may occur in CPU and external system reset. Especially, if boot ROM is reset by RSTSW#, CPU will go out of order till HAL timer shutdown, because CPU cannot read correct instruction from ROM.

Do not use RSTSW# signal for external peripherals' reset directly. If an external peripherals' reset is needed, RSTSW# signal should be masked by GPIO. This GPIO should be controlled from wake-up to HAL timer clear.



No. 18	DRAM self-refresh in hibernate mode (Direction for use)

Details

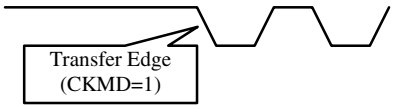
If RSTSW# is asserted during hibernate mode, DRAM may exit self-refresh and its data may be destroyed. Therefore RSTSW# should be masked by MPOWER or GPIO during hibernate mode.

No. 19	CSI - Receive Data (Direction for use)

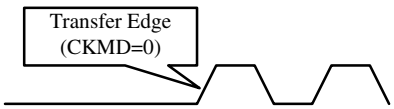
Details

The transfer must be started at the first edge of SCK clock:

1) When the SCK clock starts on falling edge, the CKMD must be set to '1'.



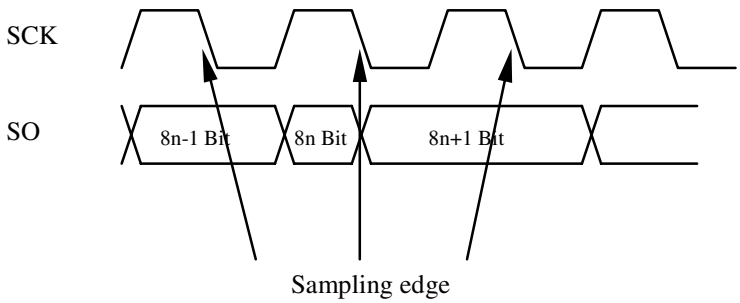
2) When the SCK clock starts on rising edge, the CKMD must be cleared to '0'.



No. 20	CSI - Send Data (Direction for use)

Details

To prevent problems for sending data, when CKMD Bit is set to 1, the SO timing of the CSI interface needs to be delayed, thus that the setup/hold time specification of the destination device is satisfied. In this mode every 8th Bit changes at the falling edge of SCK.



Note: This phenomenon does not appear, when the CKMD Bit is cleared (CKMD=0).

No. 21	Usage of mflo/mfhi instruction within branch delay slot (Direction for use)

Details
To insure proper operation of interruptions, the mflo/mfhi instruction should not be used within the branch delay slot, if the preceding instruction before the branch instruction is a div, divu, dmult, dmultu, ddiv, ddivu instruction.
Branch delay slots are activated with all Branch/Jump instructions, except beqz, bnez, bteqz and all MIPS16 branch instructions.

For example, this combination of instructions must be avoided:

```
        divu v0,v1
        bnel zero, v1, label
        mflo v0
        nop
label:  nop
        nop
```

Currently this combination of instructions is generated by applying the 'optimise platform sources'-option of Microsoft (R) C/C++ Optimizing Compiler Version 12.20.9419 for MIPS R-Series, which is delivered with WinCE V4.0 package,.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	Sept 2000	U14272EJ1V0UMJ1	VR4181 64-/32-bit Microprocessor Hardware (User's Manual)

(D) Revision History

Item	Date published	Document No.	Comment
1	January 2001	TPS-HE-B-6004-1	First release
2	April 2002	TPS-HE-B-6004-2	Added No19 and 20; Removed descriptions, which effect revisions older than Rev.1.2
3	September 2002	TPS-HE-B-6004-3	Addition of Operating Precaution No.21 Removed descriptions, which effect revisions older than Rev1.3.