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Concerned Products:	Customer Notification	Date: June 4, 1998
		NEC-Electronics (Europe) GmbH EAD –Technical Product Support
IE-789136-NS-EM1	Bug Report	Source Doc: SBG-T-0603
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June 4th, 98		Doc. No.: TPS-LE-B-ST10
1 st revision :		Doc. No.:

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(A) BUG LIST

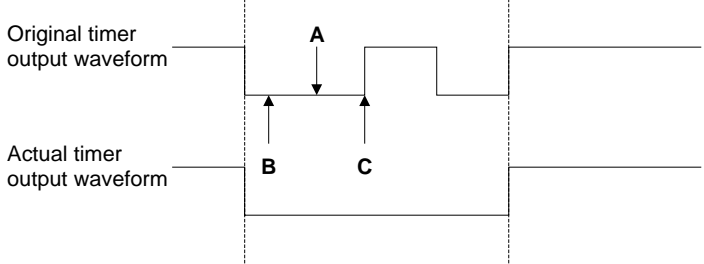
Bug No.	Outline	IE-789136-NS-EM1
1	16-bit timer / interval timer restriction	☹
2	8-bit timer / interval timer restriction	☹

- ✓: No problem
- ☹: Bug (will be corrected by next version upgrade)
- ☹: Bug (restriction, not corrected by version upgrade)

(B) BUG DESCRIPTION

Bug No.	Outline	Description
1	16-bit timer / interval timer restriction	<p>Detail: To use these timer as interval timer, be sure to carry out the following procedures before rewriting the compare register value in the coincidence interrupt routine for the count value and the 16-bit compare register (CRxx).</p> <ul style="list-style-type: none"> ① Mask interrupts ② Inhibit the timer output data inversion control (TOCxx) <p>Rewriting the value of the compare register in a state where interrupts are permitted may cause interrupt requests to occur immediately.</p>

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Bug No.	Outline	Description
2	8-bit PWM timer (TM80/TM81/TM82) restrictions	<p><u>Detail restriction 1:</u> To use these timers in interval timer mode, rewrite the value of the compare registers (CR89/CR81/CR82) in a state where the timer operation is inhibited. Rewriting the value of a compare register (CRxx) in a state where the timer operation is permitted may generate coincidence signals immediately. (In the case that interrupts are permitted, interrupt requests will occur.)</p> <p><u>Detail restriction 2:</u> These timers do not have a compare register reload function. To use them in PWM mode, therefore, rewriting the value of the compare register (CR80/CR81/CR82) during timer operation may cause the following phenomenon to occur:</p>  <p>Assuming that "B" refers to the value of the compare register (CR80/CR81/CR82) after rewriting and "C" to the value of the original compare register (CR80/CR81/CR82), an attempt to set the compare register value to "B" at the point when the counter value is "A" ($A < C$, $A > B$) will cause this cycle to fail to output the waveform.</p>