Concerned Products:	**Customer Notification**	Date: Aug. 30, 1999
		NEC-Electronics (Europe) GmbH EAD –Technical Product Support
µPD789405/6/7 µPD789415/6/7 µPD78F9418	**Bug Report**	Source Doc: SBG-T-0487 SBG-T-0524 SBG-T-0494 SBG-T-0603 SBG-T-0829 SBG-T-0995
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1st revision	: June 4th, 98	Doc. No.:	TPS-LE-B-S401
2nd revision	: Nov. 18th, 98	Doc. No.:	TPS-LE-B-S401-1
3rd revision	: Aug. 30th, 99	Doc. No.:	TPS-LE-B-S401-2

(A) BUG LIST

Bug No.	Outline	uPD78F9418				uPD789405/6/7 uPD789415/6/7	
		DS V1.0 xxxxIxxxx	DS V1.1 xxxxIxxxx	DS V2.0 NOTE 1	ES V2.1 xxxxIxxxx	DS V1.0	DS V2.0 NOTE 1
1	Serial / general purpose port switch over	✋	✋	✓	✓	✋	✓
2	Read data from UART	✋	✋	✓	✓	✋	✓
3	Flash Writing / Firmware Bug	✋	✋	✓	✓	✓	✓
4	16-bit timer / interval timer restriction	💣	💣	💣	💣	💣	💣
5	8-bit timer / interval timer restriction	💣	💣	💣	💣	💣	💣
6	STOP mode release restrictions			✋	✓	✓	✓
7	uPD78F9418A ES2.1 restrictions				💣		

✓: No problem

✋: Bug (will be corrected by next version upgrade)

💣: Bug (restriction, not corrected by version upgrade)

Note 1: uPD78F9418 (Ver. 2.0) products will be named uPD78F9418A.

(B) BUG DESCRIPTION

Bug No.	Outline	Description

1	Serial / general purpose port switch over	Details
		
		Three wire serial I/O mode
		If the operation is suspended (CSIE=0 write) while the system is transmitting/receiving data in three-wire SIO, or if the operation enable flag is cleared (CSIE=0 write) when the system is not performing transmission/reception, SO0's dual-purpose output port cannot be used as a general-purpose output port.
		
		Provisional Remedy:
		Do not clear the CSIE flag until the transmission/reception has ended. When ending the three wire SIO mode, send "FFH" first, before clearing the CSIE flag. Or, send "FFH" in the UART mode before clearing the transmission operation enable flag (TXE).
		Example 1: Three-wire SIO transmission
		MOV CSIM0, #02H
		MOV BRGC, #00H
		MOV ASIM, #00H
		MOV TXS, #0FFH
		CLR1 CSIE
		Upon writing data into TXS, the SO pin immediately turns high (after 4 clocks). However, the clocks are transmitted to the SCK clock pin.
		
		Example 2: UART transmission
		MOV CSIM0, #00H
		MOV BRGC, #00H
		MOV ASIM, #80H
		MOV TXS, #0FFH
		CLR1 TXE
		The SO pin turns Hi after 16 to 32 clocks after writing data into TXS. With this method, the SCK pin remains Low.
		
		UART mode
		If the operation is suspended (TXE=0 write) while the UART system is transmitting data, TXD's dual-purpose output port cannot be used as a general-purpose output port.
		
		Provisional Remedy:
		Do not write "0" into the transmission operation enable flag (TXE) while data is being transmitted in the transmission operation enable (TXE=1) state. When switching over to the general-purpose output port, clear the transmission operation enable flag at the point when the data transmission is completed.
		Example to switch over to the general-purpose output port after UART transmission is ended:
		
		MOV CSIM0, #00H
		MOV BRGC, #40H ; Baud rate:9600 bps
		MOV ASIM, #88H ; Data length: 8 bits; one stop bit; no parity
		WAIT:
		BF STIF, SWAIT
		CLR1 TXE

<table>
<tr><th>Bug No.</th><th>Outline</th><th>Description</th></tr>
<tr><td>2</td><td>Read data from UART</td><td>
Details
Do not read the RXB register immediately after occurrence of a reception interrupt, because an overrun error may occur.
Instead of this, wait several clock cycles as indicated in the “Clock Count Until RXB Read” table shown below, before reading RXB register!
<table>
<tr><td></td><td></td><td colspan="2">Clock Count Until RXB Read</td></tr>
<tr><td>BRGC setting</td><td>Transfer rate @ 4.9152 MHz</td><td>High speed PCCI = 0</td><td>Mid speed PCCI = 1</td></tr>
<tr><td>00H</td><td>153.6Kbps</td><td>0</td><td>0</td></tr>
<tr><td>10H</td><td>76.8Kbps</td><td>0</td><td>0</td></tr>
<tr><td>20H</td><td>38.4Kbps</td><td>0</td><td>0</td></tr>
<tr><td>30H</td><td>19.2Kbps</td><td>7</td><td>2</td></tr>
<tr><td>40H</td><td>9.6Kbps</td><td>23</td><td>6</td></tr>
<tr><td>50H</td><td>4.8Kbps</td><td>55</td><td>14</td></tr>
<tr><td>60H</td><td>2.4Kbps</td><td>119</td><td>30</td></tr>
<tr><td>70H</td><td>1.2Kbps</td><td>247</td><td>62</td></tr>
<tr><td>80H</td><td colspan="3">
In the case of an external clock, make sure that the waiting time is satisfying the following expression:

EXCL1(Hz)>f_{CPU}(Hz)/(9 clocks + X clocks)

The external clock frequency EXCL1 is “the transfer rate multiplied by 2” , f_{CPU} is the CPU’s operating frequency.
Nine clocks result because the interrupt processing is starting one clock after the occurrence of the interrupt and eight clocks are used for the interrupt processing. “X clocks” refers to the clock count until the reading is over. The timing of reading the RXB register in the interrupt routine varies from one application to another.

Example, the CPU operates at 1MHz by inputting 4.8KHz clocks from EXCK1:

4.8KHz > 1MHz/(9+X)
X > (1MHz/4.8KHz)-9
X > 199.3

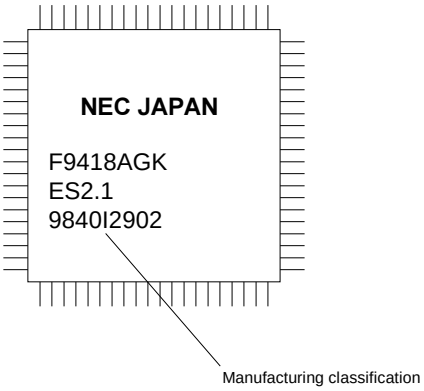
Accordingly, reading the RXB register in the interrupt routine must be performed after 200 clocks.
</td></tr>
</table>
</td></tr>
</table>

Bug No.	Outline	Description
3	Flash Writing / Firmware Bug	Details If you select one of the following modes when the flash memory is in Write mode, the P01 pin, which is a input/output port, will output the LOW level. • UART mode • Three-wire serial- I/O mode • Pseudo three-wire serial I/O mode (when using P40/P41/P42) These problems are caused by software bugs in the firmware for flash writing.

Bug No.	Outline	Description
4	16-bit timer / interval timer restriction	Detail: To use these timer as interval timer, be sure zo carry out the following procedures before rewriting the compare register value in the coincidence interrupt routine for the count value and the 16-bit compare register (CRxx). ① Mask interrupts ② Inhibit the timer output data inversion control (TOCxx) Rewriting the value of the compare register in a state where interrupts are permitted may cause interrupt requests to occur immediately.

Bug No.	Outline	Description
5	8-bit timer restriction	Detail: When using these timers, rewrite the value of the compare register (CRxx) in a state where the timer operation is inhibited. Rewriting the value of the compare register (CRxx) in a state where the timer operation is permitted may generate coincidence signals imediately. (In the case that interrupts are permitted, interrupt requests will occur.)

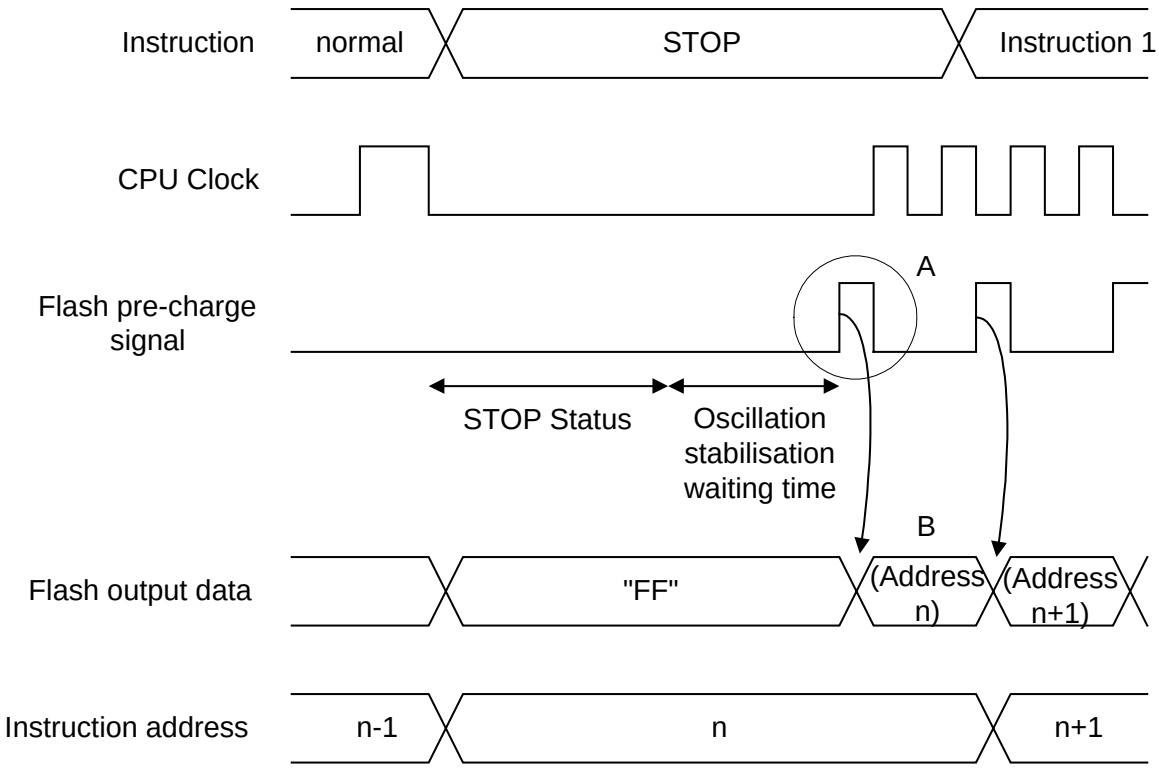
Bug No.	Outline	Description
6	Stop mode release restrictions for flash device	Detail: To use the flash device in stop mode, be sure to release the stop mode with a vector interrupt, not only with the request flag. For a detailed restriction description see the Attachment 1. An interrupt, which does not jump to a vector after stop mode is released results in runover after STOP is released.

Bug No.	Outline	Description
7	uPD78F9418A ES2.1 restrictions	Detail: 1: Restrictions The samples we are sending to your company are ES level. Therefore, NEC does not guarantee their reliability. Please use these samples for function verification only. 2: Writing to flash memory Set the flash memory write/erease VPP voltage of this product to 10.3V with the flash programmer. → As a result of this restriction, samples marked with the manufacturing classification "K" onwards should be set to VPP=10.0V. Manufacturing classification is shown on the device lot number markings as indicated below. 

Attachment 1

Example of operation where jump to vector does not occur after STOP releasing.

(When STOP instruction exists at address (n-1))



The diagram shows that the pre-charge signal does not occur and “FF” remains output since flash does not output data B.

After releasing STOP, the next instruction “Instruction 1” becomes “FF” since vector is not jumped to, and unstable operation occurs since “FF” has not been mapped.

→ When vector is jumped to after releasing STOP, data B is not used as an instruction and Instruction 1 is processed as vector operation, therefore, the problem does not occur.