Concerned Products:	**Customer Notification**	Date: November 17, 1999
		NEC-Electronics (Europe) GmbH EAD –Technical Product Support
µPD789044/6 µPD78F9046	**Bug Report**	Source Doc: SBG-T-0603 SBG-T-1641-2
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	June 26th, 98	Doc. No.:	TPS-LE-B-S046
1st revision :	August 30th, 99	Doc. No.:	TPS-LE-B-S046-1
2st revision :	Nov. 17th, 99	Doc. No.:	TPS-LE-B-S046-2

(A) BUG LIST

Bug No.	Outline	µPD789044/6	µPD78F9046
1	16-bit timer / interval timer restriction	💣	💣
2	8-bit timer / interval timer restriction	💣	💣
3	16-bit timer 90 restriction	💣	💣

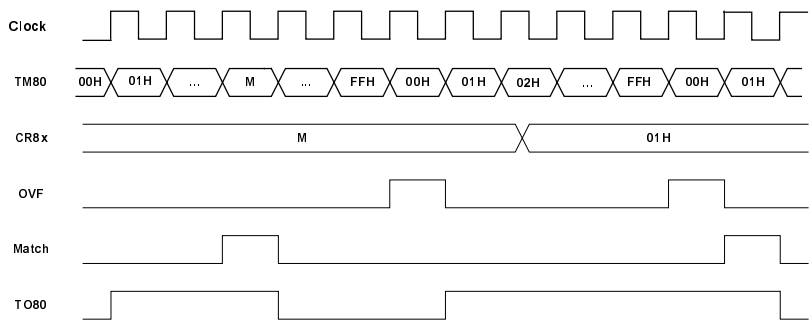
✓: No problem

✋: Bug (will be corrected by next version upgrade)

💣: Bug (restriction, not corrected by version upgrade)

(B) BUG DESCRIPTION

Bug No.	Outline	Description
1	16-bit timer / interval timer restriction	Detail: To use these timer as interval timer, be sure to carry out the following procedures before rewriting the compare register value in the coincidence interrupt routine for the count value and the 16-bit compare register (CRxx). ① Mask interrupts ② Inhibit the timer output data inversion control (TOCxx) Rewriting the value of the compare register in a state where interrupts are permitted may cause interrupt requests to occur immediately.

Bug No.	Outline	Description
2	8-bit PWM timer (TM80/TM81/TM82) restrictions	Detail restriction 1: To use these timers in interval timer mode, rewrite the value of the compare registers (CR89/CR81/CR82) in a state where the timer operation is inhibited. Rewriting the value of a compare register (CRxx) in a state where the timer operation is permitted may generate coincidence signals immediatley. (In the case that interrupts are permitted, interrupt requests will occur.) Detail restriction 2: These timers do not have a compare register reload function. To use them in PWM mode, therefore, rewriting the value of the compare register (CR80/CR81/CR82) during timer operation may cause the following phenomenom to occur: If a value is written to a compare register (CR8x), a high level may be output for the next one cycle (count pulse x 256). This phenomenon occurs only if a value smaller than the value of TM8x is written to CR8x. 

Bug No.	Outline	Description
3	16-bit timer 90 restriction	When this timer is used under the following conditions, the timer output function and timer interrupt function cannot be used. Condition: Timer clock: Subclock fXT CPU clock: Subclock fXT Main clock: Stopped BZOE90 : “0” (no buzzer output) Measures if the main clock is stopped to lower the current consumption and subclock is selected as the clock of this timer to release the halt mode. Perform the following settings: Timer clock: Subclock fXT CPU clock: Subclock fXT Main clock: Stopped BZOE90 : “1” (buzzer output enabled) When the port mode register and output latch of a pin are multiplexed with buzzer output are”0”, a waveform is output from multiplexed pin. To take the above measures, take either of the following measures: - Set the buzzer output multiplexed pin in input mode. – If the buzzer output multiplexed pin cannot be set in the input mode, set the value of the port latch to “1”. (The buzzer output multiplexed pin output “H”). This operation is explained in detail on **Attachement 1**

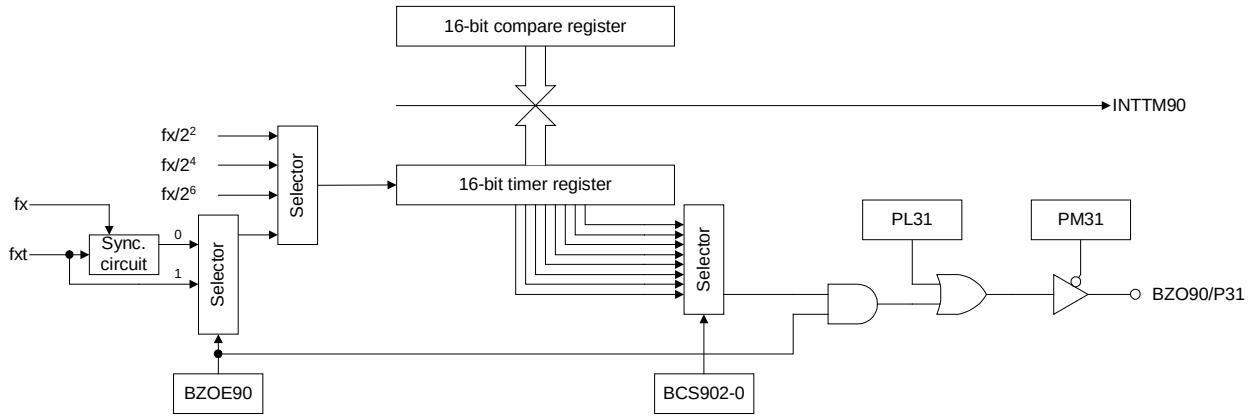
Attachement 1

The following table shows the operation to be performed in each timer operation status.

	Count Clock	CPU Clock	System Clock		BZOE90	Capture	TM90 Read	Buzzer Output	Timer Output	Timer Interrupt
			Main clock	Sub clock						
(1)	$fx/2^2$, $fx/2^6$, $fx/2^7$	Main	Oscillation	Oscillation /stop	1/0	O	O[Note]	O/X	O	O
(2)		Sub	Oscillation	Oscillation		O	X	O/X	O	O
(3)			Stop	Oscillation		X	X	X	X	X
(4)	fxt	Main	Oscillation	Oscillation	0	O	O	X	O	X
(5)					1	X	X	O	O	O
(6)				Stop	1/0	X	X	X	X	X
(7)			Stop (STOP mode)	Oscillation	0	X	X	X	X	X
(8)					1	X	X	O	O	O
(9)				Stop	1/0	X	X	X	X	X
(10)		Sub	Oscillation	Oscillation	0	O	O	X	O	O
(11)					1	X	X	O	O	O
(12)			Stop		0	X	X	X	X	X
(13)					1	X	X	O	O	O

O…Operable, **O/X**…Depends on BZOE90, **X**…Inoperable
Note Possible only when CPU clock is in high-speed mode

[Reason that interrupt and timer output are not operable in condition (12) above]
If the subclock is selected as timer clock with BZOE90= "0" as shown in the following block diagram, the subclock synchronized with the main clock is selected as the count clock of the 16-bit timer register. If the main clock is stopped at this time, therefore, the subclock is also stopped. As a result, the timer does not operate (neither does an interrupt occur).



Block Diagram of 16-bit Timer