Concerned Products:	**Customer Notification**	Date: 16 August 2000 NEC-Electronics (Europe) GmbH EAD –Technical Product Support
μPD784214 ***μPD784214Y*** ***μPD784215*** ***μPD784215Y*** ***μPD784216*** ***μPD784216Y*** ***μPD78F4216*** ***μPD78F4216Y*** ***μPD784214A*** ***μPD784214AY*** ***μPD784215A*** ***μPD784215AY*** ***μPD784216A*** ***μPD784216AY*** ***μPD78F4216A*** ***μPD78F4216AY*** ***μPD784217*** ***μPD784217Y*** ***μPD784218*** ***μPD784218Y*** ***μPD78F4218*** ***μPD78F4218Y*** ***μPD784217A*** ***μPD784217AY*** ***μPD784218A*** ***μPD784218AY*** ***μPD78F4218A*** ***μPD78F4218AY***	**Bug Report**	Source Doc: SBG-T-0483 SBG-T-0504 SIF-T-?? (TQ-TH970820/1) SIF-T-10395 (TQ-TH971215/2) SBG-T-0619 SBB-T-12655 SBG-T-2079 SBG-T-13641 NN Author: A. Twardy
Date of initial issue:	5th Feb. 98	Doc. No.: TPS-LE-B-4217

(A) BUG LIST

Bug No.	Outline		μPD784214 Note4 μPD784214Y				μPD784215 Note4 μPD784215Y				μPD784216 Note4 μPD784216Y				μPD78F4216 μPD78F4216Y					
		Rev.	1.0				2.0	2.2			2.0	2.2			ES1.0	ES1.1	ES2.1	ES2.4	2.1	2.4
		Standard	K	E			K	E			K	E	P		I	I	I	I	K	E
1	IDLE mode release		☝	☝			☝	☝	☝		☝	☝	☝		☝	☝	☝	☝	☝	☝
2	ADC initial conversion result		💣	💣			💣	💣	💣		💣	💣	💣		💣	💣	💣	💣	💣	💣
3	ADC conversion result after stop		💣	💣			💣	💣	💣		💣	💣	💣		💣	💣	💣	💣	💣	💣
4	I2C restart procedure Note1		☝	☝			☝	☝	☝		☝	☝	☝		☝	☝	☝	☝	☝	☝
5	Low power consumption mode Note2		✓	✓			✓	✓	✓		✓	✓	✓		☝	☝	☝	☝	☝	☝
6	TIMER compare register access Note3		☝	☝			☝	☝	☝		☝	☝	☝		☝	☝	☝	☝	☝	☝
7	Restrictions and remarks		✓	✓			✓	✓	✓		✓	✓	✓		☝	☝	☝	☝	☝	☝

✓: No problem
☝: Bug (will be corrected by version upgrade)
💣: Bug (restriction, not corrected by version upgrade)

Note1: Applicable for μPD784216Y subseries only.

Note2: In 78F4216A/F4216AY, it will be corrected.

Note3: In 784214A/4215A/4216A/F4216A, it will be corrected.

Note4: The actual Mask-Level of the devices will be given in the next version of the Bug Report. In case of unclearness please ask NEC-EE EAD-TPS

*) For the Revision History please refer to point (C)

Bug No.	Outline		μPD784214A Note2 μPD784214AY				μPD784215A Note2 μPD784215AY				μPD784216A Note2 μPD784216AY				μPD78F4216A μPD78F4216AY								
		Rev.	1.0				1.0				1.0				ES1.0	ES1.1	ES1.2	CS	CS	ES1.6	ES2.6	ES3.1	CS3.1
		Standard	K				K				K				I	K	E	K	E	P	P	X	X
1	IDLE mode release		✓	✓			✓	✓			✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
2	ADC initial conversion result		💣	💣			💣	💣			💣	💣			💣	💣	💣	💣	💣	💣	💣	💣	💣
3	ADC conversion result after stop		💣	💣			💣	💣			💣	💣			💣	💣	💣	💣	💣	💣	💣	💣	💣
4	I2C restart procedure Note1		✓	✓			✓	✓			✓	✓			✋	✋	✓	✋	✓	✓	✓	✓	✓
5	Low power consumption mode		✓	✓			✓	✓			✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓
6	TIMER compare register access		Note3 ✓	Note3 ✓			Note3 ✓	Note3 ✓			Note3 ✓	Note3 ✓			✋	✋	Note3 ✓	✋	Note3 ✓	Note3 ✓	Note3 ✓	Note3 ✓	Note3 ✓
7	Restrictions		✓	✓			✓	✓			✓	✓			✋	✋	✋	✋	✋	✋	✋	✋	✋

✓: No problem
✋: Bug (will be corrected by version upgrade)
💣: Bug (restriction, not corrected by version upgrade)

Note1: Applicable for μPD784216AY subseries only.

Note2: The actual Mask-Level of the devices will be given in the next version of the Bug Report. In case of unclearness please ask NEC-EE EAD-TPS

Note3: 3.1 To rewrite the compare register when the 8-Bit timers are cascaded, stop both the high-order and the low-order timer.

3.2. If the compare register is read while the 8-bit timer is used in the PWM mode the value written to the master register is read. The compare register has a double buffer configuration, consisting of a master and a slave register. A value set in the program to the compare register is written to the master register. This value is loaded from the master register to the slave register if the value of the timer coincides with that of the slave register. Therefore the compare value is read from the master register to establish coincidence at the next timing.

Bug No.	Outline		μPD784217 Note2 μPD784217Y				μPD784218 Note2 μPD784218Y				μPD78F4218 μPD78F4218Y			
		Rev.	1.0				1.0				ES1.101	ES1.123	ES1.2	
		Standard	K				K				I	I	I	
1	IDLE mode release		✋				✋				✋	✋	✋	
2	ADC initial conversion result		💣				💣				💣	💣	💣	
3	ADC conversion result after stop		💣				💣				💣	💣	💣	
4	I2C restart procedure Note1		✋				✋				✋	✋	✋	
5	Low power consumption mode		✓				✓				✋	✋	✋	
6	TIMER compare register access		✋				✋				✋	✋	✋	
7	Restrictions		✓				✓				✋	✋	✋	

✓: No problem
✋: Bug (will be corrected by version upgrade)
💣: Bug (restriction, not corrected by version upgrade)

Note1: Applicable for μPD784218Y subseries only.

Note2: The actual Mask-Level of the devices will be given in the next version of the Bug Report. In case of unclearness please ask NEC-EE EAD-TPS

Bug No.	Outline		μPD784217A Note1 μPD784217AY				μPD784218A Note1 μPD784218AY				μPD78F4218A μPD78F4218AY			
		Rev.									ES1.4	CS1.4	CS1.4	
		Standard									K	K	E	
1	IDLE mode release		✓				✓				✓	✓	✓	
2	ADC initial conversion result		💣				💣				💣	💣	💣	
3	ADC conversion result after stop		💣				💣				💣	💣	💣	
4	I2C restart procedure		✓				✓				✓	✓	✓	
5	Low power consumption mode		✓				✓				✓	✓	✓	
6	TIMER compare register access		Note2 ✓				Note2 ✓				Note2 ✓	Note2 ✓	Note2 ✓	
7	Restrictions		✓				✓				✋	✋	✋	

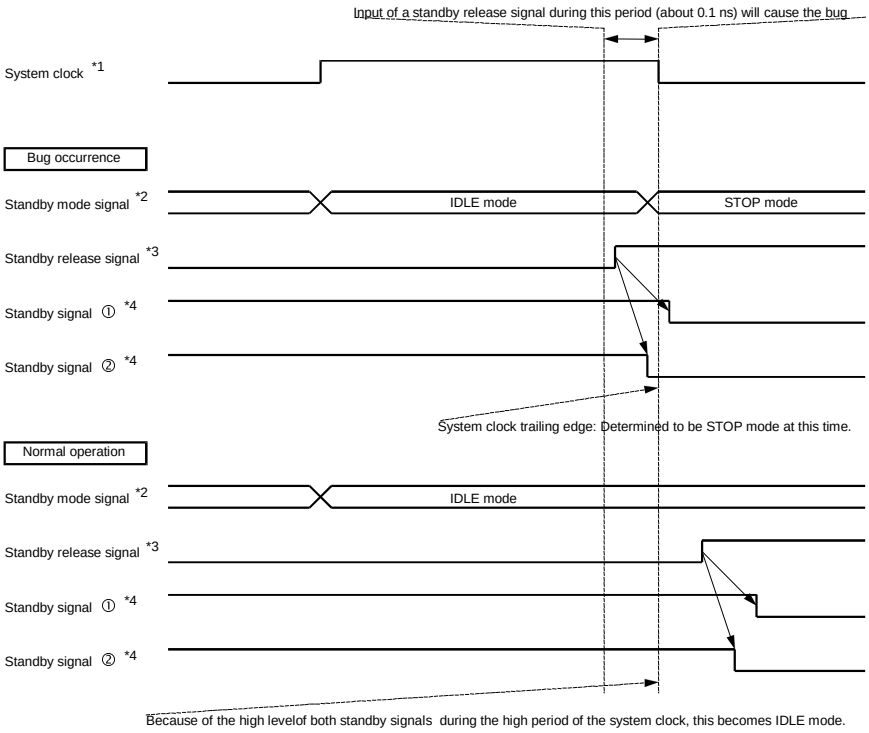
✓: No problem
✋: Bug (will be corrected by version upgrade)
💣: Bug (restriction, not corrected by version upgrade)

Note1: The actual Mask-Level of the devices will be given in the next version of the Bug Report. In case of unclearness please ask NEC-EE EAD-TPS

Note2: 2.1 To rewrite the compare register when the 8-Bit timers are cascaded, stop both the high-order and the low-order timer.

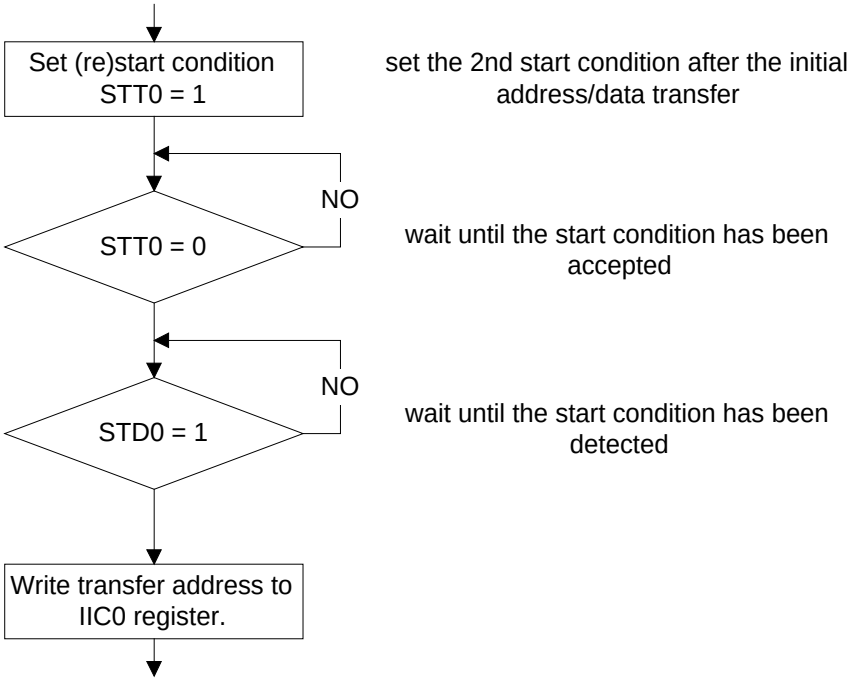
2.2. If the compare register is read while the 8-bit timer is used in the PWM mode the value written to the master register is read. The compare register has a double buffer configuration, consisting of a master and a slave register. A value set in the program to the compare register is written to the master register. This value is loaded from the master register to the slave register if the value of the timer coincides with that of the slave register. Therefore the compare value is read from the master register to establish coincidence at the next timing.

(B) BUG DESCRIPTION

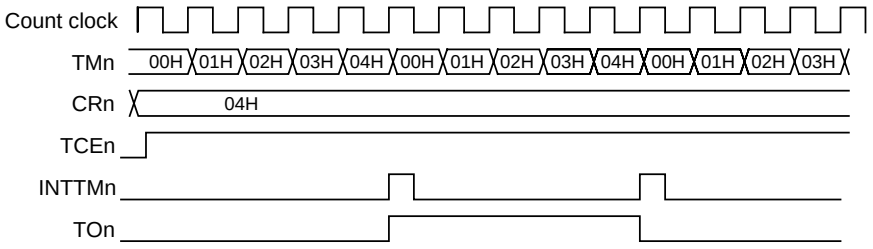
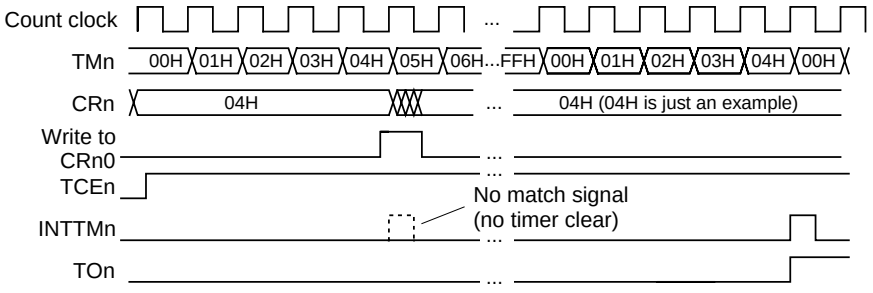
Bug No.	Outline	Description
1	Cancelling the IDLE mode may cause a wait during the oscillation stabilization time that has been set by oscillation stabilization time specification register (OSTS).	*Details* When a contention occurs between the execution of an IDLE mode instruction and an interrupt to release the IDLE mode, STOP mode is released after executing STOP mode, rather than IDLE mode being released after executing IDLE mode as it should. Therefore, despite the fact that the program has set the IDLE mode, this bug results in a wait for the length of oscillation stabilization time that is set by the oscillation stabilization time register (OSTS), when cancelling this mode. Normally, when cancelling the IDLE mode, there is no need to wait for the duration of the oscillation stabilization time. Specifically, when the bug occurs, an operation as shown in the following timing chart is performed.  *1: Internal system clock *2: The signal notifying entry to entering each standby mode, While the system clock is high, the values of standby signals ① and ② are latched, and signals to select which standby mode to enter are created. *3: The standby mode release signal created by the microprocessor by inputting the standby mode release factor. *4: STOP mode: Signal ① = 1, Signal ② = 0 HALT mode: Signal ① = 0, Signal ② = 1 IDLE mode: Signal ① = 1, Signal ② = 1

Bug No.	Outline	Description
1	(continuation)	*Description of timing chart* First, standby signal ① and ② is changed by executing the IDLE instruction. Then, while the system clock has high level, the values of standby signals are latched. Selection of the standby mode to enter is set by falling edge of the system clock. The standby mode signal is placed in IDLE mode if the standby signals ① and ② are high level respectively while the system clock is high. The bug is generated when the standby mode release interrupt occurs after the standby mode instructions (MOV STBC, #byte) and immediately before the falling edge of the initial system clock. Because of the time difference generated after the standby release interrupt until the signals ① and ② are cleared, the system is placed in the STOP mode signal status when the system clock falls, which is neither IDLE mode nor normal mode. Consequently, the system is determined to be in the STOP mode, thus resulting in the wait for the duration of oscillation stabilization time upon cancellation of the standby. *Workaround* Unfortunately, it is impossible to take perfect countermeasures in software. As it was explained above, in order to stop this bug from occurring, it is necessary to make sure that the external interrupts and input to the IDLE instruction do not conflict with each other. So it is recommended, when using the IDLE mode, to **shorten the value of the oscillation stabilization time**, which is set by the OSTS register. This bug doesn't occur unless an external interrupt is generated during the short time of about 0.1 ns when executing the IDLE instruction. Therefore, the rate of occurrence is considered extremely low.

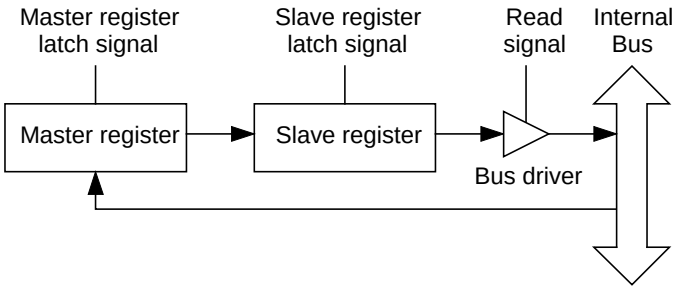
Bug No.	Outline	Description
2	The initial conversion result immediately after the A/D conversion operation startup may not satisfy the specification.	*Details* Immediately after the A/D conversion is started, the reference voltage of the A/D converter is unstable. The normal operation of the sampling circuit being controlled is affected by this voltage, thus increasing the conversion error. Because the conversion error at this time cannot be confirmed due to differences in conversion speed and uneven product quality, etc., the conversion result becomes an undefined value. *Workaround* Do not use the initial result (contents of ADCR register) immediately after the A/D converter is started. Instead, use the second or later conversion results subsequently generated (ref. to the diagram below). When the A/D conversion end interrupt (INTAD) of the initial conversion occurs, either accept it or clear the appropriated interrupt request flag ADIF.
3	If the conversion result is read after halting the A/D conversion operation, the value may be undefined.	*Details* If the timing for the A/D conversion end conflicts with that for halting the A/D conversion operation, an undefined value is stored into the ADCR. Reading the conversion result afterwards will result in reading an undefined value. *Workaround* Read the A/D conversion result register ADCR while the A/D converter is operating. When reading the conversion result after halting the A/D conversion, make sure that timing for halting A/D conversion does not conflict with that for the end of the A/D conversion.

Bug No.	Outline	Description
4	Using the I^2C restart condition causes a faulty address transfer.	*Details* If the transfer address is set to the shift register (IIC0) immediately after the (re)start is set (STT = 1), the transfer address will be sent simultaneously by rising edge of the serial clock (SCL). The serial clock is at low level normally before a restart condition will be set, due to the preceded address/data transfer. To generate a (re)start condition the serial clock (SCL) has to be first on high level (recessive state). By falling edge of the SDA line, when SCL has high level, the (re)start condition can be detected. Afterwards the SCL line will fall to low level and the slave address can be transferred by normal operation. Now, if the slave address is written into the shift register (IIC0) immediately after the start condition trigger (STT0) is set, the rising edge on the SCL line resulting in data output before the start condition is set. This causes the bug. *Workaround* The transfer address must be set after the confirmation of start condition detection (STT=0, STD = 1). 

Bug No.	Outline	Description
5	The low power consumption mode, where the device operates by sub-system clock, cannot be used.	*Details* Only flash devices are concerned by this bug. The problem is caused by the integrated charging pump, which is needed for reading the flash memory. At higher temperature a malfunction occurs, and the CPU cannot fetch the program code from the flash memory correctly. Therefore the program execution becomes undefined. *Workaround* No. Do not use the low power consumption mode for flash devices. Just the operation at room temperature (about 25°C) is permitted, in order to carry out an evaluation for revised devices.

Bug No.	Outline	Description
6	Timer compare register access while corresponding timer register matches	*Details* The Bugs described below concern all 8-Bit Timers of the µPD784216/4216Y subseries. In detail the timers concerned are Timer 1, 2, 5, 6, 7 and Timer 8. 6.1 Interval timer mode Writing to a compare register while the corresponding timer register matches does not generate an interrupt request. Under conditions like above the timer register is not cleared in the “Timer Clear & Start” mode. 6.2 Square wave output mode Writing to a compare register while the corresponding timer register matches does not invert the output signal of the timer output. Please refer to the timing diagrams shown below. Please note, however, that the timing charts below are schematic representations of operations and therefore do not indicate a precise operation timing. *Normal operation*  Please note, however, that the timing charts below are schematic representations of operations and therefore do not indicate a precise operation timing. *Bug occurrence (6.1 and 6.2)* 
6	Timer compare register	6.3 PWM output mode

Bug No.	Outline	Description
	access while corresponding timer register matches (continuation)	The compare registers of the concerned timers consist of two buffers the master and the slave register. The simplified diagram is show below.



In PWM mode the data transfer from the master to the slave register is performed when an overflow occurs. This bug occurs when performing a data transfer from the concerned master register to the slave register when an overflow occurs in an attempt to rewrite the value of the master register, thus damaging the data to be transferred.

The description of the bugs are in detail as following:

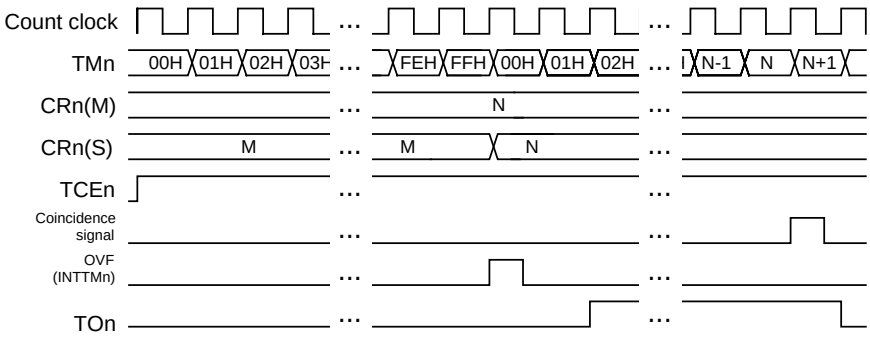
6.3.1 Writing to a compare register while the corresponding timer register matches does not change the output signal of the timer to the inactive level.

6.3.2 Writing to CRn0 (master register) once and then writing again when the corresponding timer register (TMn) overflows causes an undefined value to be transferred to CRn0 (slave register).

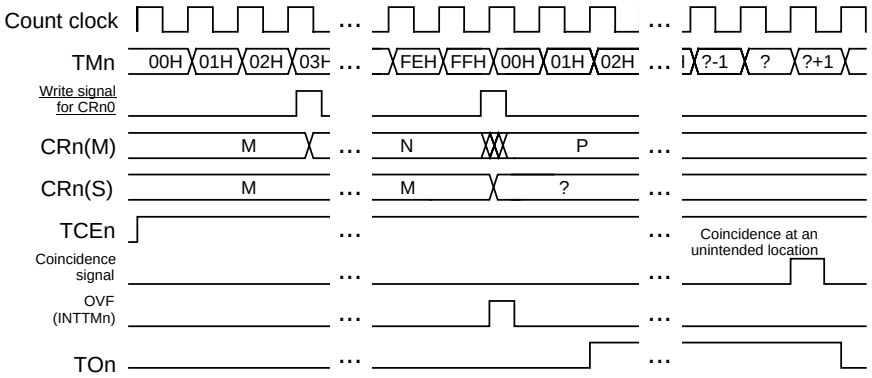
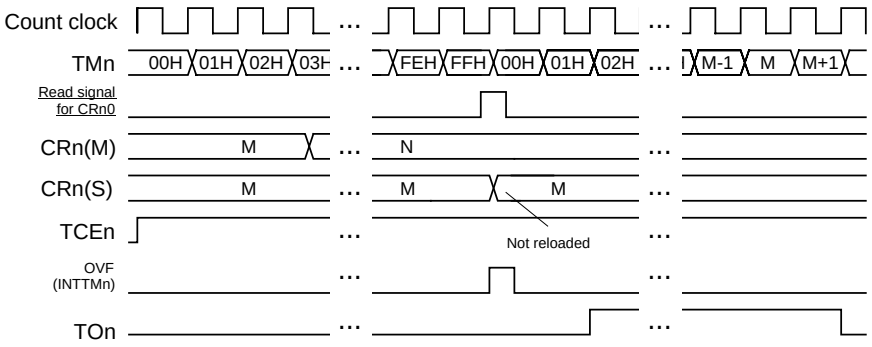
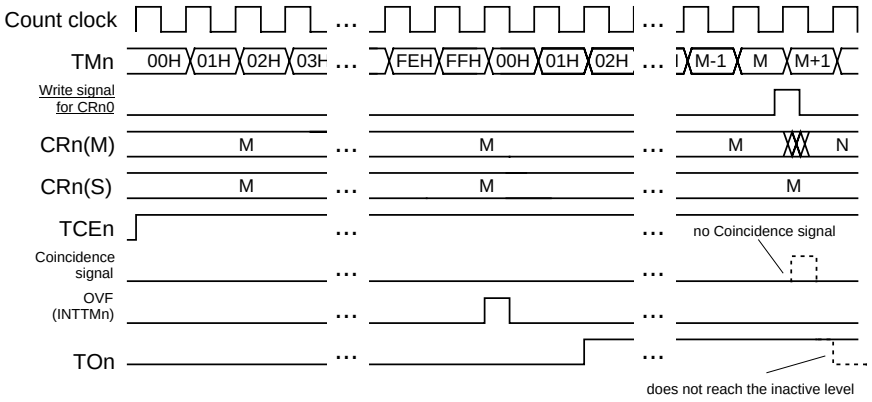
6.3.3 Reading the compare register when an overflow of the corresponding timer occurs stops the transfer of data form CRn0 (master register) to CRn0 (slave register). The transfer is performed when overflow of the timer occurs.

Please refer to the timing diagrams shown below.

Normal operation as PWM timer



6	Timer compare register access while corresponding timer	*Bug occurrence in PWM timer mode (6.3.1)*

Bug No.	Outline	Description
	register matches (continuation)	 *Bug occurrence in PWM timer mode (6.3.2)*  *Bug occurrence in PWM timer mode (6.3.3)* 
6	Timer compare register access while corresponding timer register matches	*Workaround* In general the countermeasure is to avoid writing to the compare register by coincedence between timer register and compare register. This can be

Bug No.	Outline	Description
	(continuation)	realised by using the interrupt processing (INTTMn) of each timer. In the cases mentioned under 6.1 and 6.2 Use the interrupt which is generated by coincedence between the timer register and the compare register. This interrupt should be used to write to the compare register before the next coincedence occurs. In the cases mentioned under 6.3.1, 6.3.2 and 6.3.3 Use the interrupt which is generated when the overflow of the timer occurs. In this interrupt process avoid the correspondences between the timer register, the compare register and the next timeroverflow. Another countermeasure for all bugs mentioned under 6, is to stop the timer operation once before resuming it.

Bug No.	Outline	Description
7	Restrictions and remarks	*7.1 Details* Only the devices with on-chip flash memory are concerned by these restrictions. 7.1.1 All devices with on-chip flash memory need a PREWRITE with 00 (HEX) before erasing can be performed. Single Block operation is not guaranteed. Please note, that the operation at 24 hours a day of the devices is not guaranteed. The limitation of not guaranteed 24 hours operating a day will be removed by version upgrade 7.1.2 Devices 78F4216/18(Y) with revisions ES1.0, ES1.1, ES1.101, ES1.123, ES1.2, ES2.1, ES2,4 Operating temperature: -10 to +60 deg C Programming temperature: +10 to +40 deg C Operating voltage: 2.7V to 5.5V Programming voltage: 10V +/- 0.3V Programming cycles in a row: 3 Number of W/E cycles: 5 but no guarantee for ES-samples Data retention: 10 years but no guarantee for ES-samples subclock: not working correctly 7.1.3 Devices 78F4216A(Y) with revisions ES1.0, ES1.1, CS (RANK "K") Operating temperature: -10 to +60 deg C (Flashmacro 6.5) Programming temperature: +10 to +40 deg C Operating voltage: 2.7V to 5.5V Programming voltage: 10.3V +/- 0.3V Programming cycles in a row: 1 *) Number of W/E cycles: 5 times but no guarantee for ES-samples Data retention: 10 years but no guarantee for ES-samples ECC function: not implemented on chip 7.1.4 Devices 78F4216A(Y) with revisions ES1.2 and CS (RANK "E") Operating temperature: -40 to +85 deg C (Flashmacro 7.0, 7.1) Programming temperature: +10 to +40 deg C Operating voltage: 2.2V to 5.5V Programming voltage: 10.0V +/- 0.3V Programming cycles in a row: 1 *) Number of W/E cycles: 20 but no guarantee for ES-samples Data retention: 10 years but no guarantee for ES-samples 7.1.5 Devices 78F4216A(Y) with revisions ES1.6 and ES2.6 Operating temperature: -40 to +85 deg C (Flashmacro 7.7) Programming temperature: +10 to +40 deg C Operating voltage: 1.9V to 5.5V Programming voltage: 10.0V +/- 0.3V Programming cycles in a row: 1 *) Number of W/E cycles: 20 but no guarantee for ES-samples Data retention: 10 years but no guarantee for ES-samples

Bug No.	Outline	Description
7	Restrictions and remarks (continuation)	7.1.6 Devices 78F4216A(Y) with revision ES3.1 Operating temperature: -40 to +85 deg C (Flashmacro 8.5) Programming temperature: +10 to +40 deg C Operating voltage: 1.9V to 5.5V Programming voltage: 10.0V +/- 0.3V Programming cycles in a row: 1 *) Number of W/E cycles: 20 but no guarantee for ES-samples Data retention: 10 years but no guarantee for ES-samples 24 hours operating: no guarantee due to ES-samples writeback-function: is needed 7.1.7 Devices 78F4216A(Y) with revisions CS3.1 (RANK "X") Operating temperature: -40 to +85 deg C (Flashmacro 8.5) Programming temperature: +10 to +40 deg C Operating voltage: 1.9V to 5.5V Programming voltage: 10.0V +/- 0.3V Programming cycles in a row: 1 Number of W/E cycles: 20 Data retention: 10 24 hours operating: guaranteed writeback-function: is needed 7.1.8 Devices 78F4218A(Y) with revisions ES1.4 (RANK "K") Operating temperature: -40 to +85 deg C (Flashmacro 8.2) Programming temperature: +10 to +40 deg C Operating voltage: 1.9V to 5.5V Programming voltage: 10.0V +/- 0.3V Programming cycles in a row: 1 *) Number of W/E cycles: 20 but no guarantee for ES-samples Data retention: 10 years but no guarantee for ES-samples 24 hours operating: no guarantee due to ES-samples writeback-function: is needed 7.1.9 Devices 78F4218A(Y) with revisions CS1.4 and the RANK "K" or the RANK “E” Operating temperature: -40 to +85 deg C (Flashmacro 8.2) Programming temperature: +10 to +40 deg C Operating voltage: 1.9V to 5.5V Programming voltage: 10.0V +/- 0.3V Programming cycles in a row: 1 Number of W/E cycles: 20 Data retention: 10 24 hours operating: guaranteed writeback-function: is needed *) Two times programming is only needed if the first programming is not successful.

Bug No.	Outline	Description
7	Restrictions and remarks (continuation)	*7.2 Details concerning Flashprogramming* 7.2.1 Remarks using FlashProII For programming the following devices a **FlashPro*II*** version **2.35 or higher** is needed, due to a change in the programming sequence. Devices: 78F4216A(Y) with the revisions ES1.0, ES1.1, ES1.2 and CS (with rank K and E) 7.2.2 Remarks using FlashMaster (for all version lower than V2.00) For programming the following devices a **FlashMaster** version **2.00 or higher** is needed, due to a change in the programming voltage (10.3V). Devices: 78F4216A(Y) with the revisions ES1.0, ES1.1 and CS (with rank K) 7.2.3 Restrictions using FlashMaster V2.00 For programming the following devices a **FlashMaster** version **V2.00 can only be used with restrictions**. Devices: **78F4218A (Y) revision ES1.4 and devices 78F4216A(Y) revision ES3.1**. The restrictions are caused by some changes in the programming algorithm. If the FlashMaster V2.00 is used to program the devices above the correct programming can not be guaranteed. For testing and evaluation purpose only the devices may be erased by using the block-mode, therefore the EPV command can not be used. Erasing, programming and verifying has to be performed manually. Please, do not use the writeback-function of the FlashMaster V2.00 due to incorrect implementation. 7.2.4 For devices the devices 78F4216A(Y) CS3.1 and 78F4218A(Y) CS1.4 For programming the devices mentioned above a FlashMaster V3.00 or higher is needed to program the devices correctly. *Workaround* For all restrictions listed under point 7.x.x there are no workarounds.

(C) Revision history

No.	Outline	Description	
1.	Updates from Doc. No.: TPS-LE-B-4215 to Doc.-No: TPS-LE-B-4216	1.1.1	Correction of typing error concerning point 7.1.9. The expression "(RANK "E")" was replaced by "(RANK "K")".
		1.1.2	Correction of typing error concerning the overview table on page 5. The standard of 78F4218A CS1.4 was changed from E to K.
		1.2	The explanation concerning the "24-hour operating" was adapted.
2.	Updates from Doc. No.: TPS-LE-B-4216 to Doc.-No: TPS-LE-B-4217	1.1	Addition of 78F4218A devices with the RANK “E” related to point 7.1.9.
		1.2	Correction of “24-hour operating” limitation due to new test results, related to point 7.1.9.
		1.3	Correction of the BUG described under point 1 of the BUG LIST (1. Idle mode release). The bug has been removed on all A-Type devices of the 78421xA series.