Concerned Products:	**Customer Notification**	Date: November 18, 1998
IE-78078-R-EM		NEC-Electronics (Europe) GmbH EAD – Technical Product Support
	Bug Report	Source Doc: SBG-T-0819
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(A) BUG LIST (1/2)

Bug No.	Outline	IE-78078-R-EM			
		V1.00 Level “A”	V1.10 Level “B”	V1.21 Level “C”	V1.22 Level “D”
1	Latch-up P4, P5, P6	💣	✋	✓	✓
2	External memory mode	💣	✋	✓	✓
3	External sense clips	✋	✓	✓	✓
4	Interrupt of UART	💣	💣	✋	✓
4	Operation as slave in IIC mode	💣	💣	💣	💣

✓: No problem

✋: Bug (will be corrected by next version upgrade)

💣: Bug (restriction, not corrected by version upgrade)

(B) BUG DESCRIPTION

Bug No.	Outline	Description
1	Latch-up P4, P5, P6	If two or more pins from P4, P5 and P6 are reset when suspended on 5V-power supply, the latch-up circuit operates.
2	External memory mode	The ASTB/!RD/!WR signals are not output when the external memory mode is used.
3	External sense clips	The external sense clips can not be used when the probe for the 7808x series is used.
4	Interrupt of UART	With the 78K/0 series serial interface channel 2 UART function, after serial transmission is completed, transmission may not be performed even though the next transmission start instruction is executed. This is because, after the serial transmission completion interrupt (INTST signal) has been generated. The next transmission start instruction (write to TXS) is not acknowledged for a certain period. The period during which a transmission start instruction is not acknowledged is one cycle of the reference clock used for serial transfer control. When the dedicated baud rate generator output is used, this reference clock is determined by the 4 bits TPS3 to TPS0 of the baud rate generator control register and the MCS bit of the oscillation mode selection register (OSMS). If a clock is supplied to the ASCK pin from off-chip, that external clock is used as the reference clock. There is no problem with operation as a normal 3-wire serial interface or the UART receive operation. <u>Workaround</u> Wait processing should be inserted by means of a software timer between generation of the serial transmission completion interrupt (INTST) and execution of the next transmission starts instruction (write to TXS). The length of this time should be as follows: *When the dedicated baud rate generator is used:* Longer than the time calculated from the expression given in the preceding table. *When the clock is supplied to the ASCK pin from off-chip:* Longer than one cycle of the supplied clock.

5	Operation as slave in IIC mode	When the serial interface channel is used as slave of the IIC bus mode and the wake-up is executed (the function is executed by WUP -> 1) in the serial transfer state (**Note1**). The address is determined to data between the other slave and the master. When the data matches with the slave address, the device participates in communication and the communication data is disrupted. There will be no modification of these limitation. **Note1**: The serial transfer state means the state until the end of the serial transfer sets CSIIFO after the shift register (SIO0) is written. Workaround The problems can be avoided by changing software. Before executing the wake-up function, run the software which releases the serial transfer state as shown in the below example. Further, during the wake-up function is executed, do not write data into the shift register. Software which releases the serial transfer mode The following software releases the serial transfer mode. In order to release the serial transfer state, the serial interface channel 0 must be set the operation halt state (CSIE0 -> 0). However, when the serial interface channel is set into halt state in the IIC bus mode, high level is output on the SCL pin and low level is output on the SDA pin. Due to this the communication on the IIC bus may be affected. The following software is for the case, in which Pin P25 is used as serial data bus. When P26 is used as serial data bus, change PM2.5 and P2.5 to PM2.6 and P2.6. SET1 P2.5; Low level is not output from the SDA pin when the system returns to the IIC mode by the instruction SET1 CSIE0 (The state of output from the SDA pin is set to Hi-Z by this instruction). SET1 PM2.5; The P25 pin (SDA) is set to input mode so that the SDA line may not be affected when the system enters the port mode by the instruction CLR1 CSIE0. SET1 PM2.7; The P27 pin (SCL) is set to input mode so that the SCL line may not be affected when the system enters the port mode by the instruction CLR1 CSIE0 (The input mode is set at the time when the instruction CLR1 CSIE0 is executed). CLR1 CSIE0; The IIC mode is changed into port mode. SET1 CSIE0; The port mode is changed into IIC mode.

		SET1 RELT; Low level is not output from SDA pin by the instruction CLR1 P2.5 CLR1 PM2.7; Since P27 pin needs to be set to output mode in the IIC mode, the P27 pin is set to the output mode. CLR1 P2.5; Since “0” is set to the output latch of the P25 pin in the IIC mode, “0” is set to it. CLR1 PM2.5; Since the P25 pin needs to set the output mode in the IIC mode, the P25 pin is set to output mode Further, when CSIE0=0, that the flags which are shaded are cleared. SBIC BSYE ACKD ACKE ACKT CMDD RELD CMDT RELT