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Concerned Products:	Customer Notification		Date: March 2nd, 1999		
16F15 1615 1616			NEC-Electronics (Europe) GmbH EAD -Technical Product Support		
	Bug Report		Source Doc: EEUD-BR-0001 (TM5 – interrupt)		
			Author: A. Wohlfahrt		
			Date of initial issue: Jan. 21 st , 99		Doc. No.: TPS-LE-B-01615
			1 st revision : Mar. 2 nd , 99		Doc. No.: TPS-LE-B-01615-1
	2 nd revision :		Doc. No.:		
3 rd revision :		Doc. No.:			

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(A) BUG LIST

Bug No.	Outline	uPD16F15					uPD1615 / 1616	
		ES V1.0 xxxxlnnnn	CS V1.0 xxxxKnnnn				ES1.0	
1	Flash memory characteristics	☛	☞				no Flash	
2	AD Converter	☛	☛				☛	
3	VAN UDL	☛	☞				☞	
4	Timer 5n – data match	☛	☞				☞	
5	Timer 5n – interrupt	☛	☞				☞	

✓: No problem

☞: Bug (will be corrected by next version upgrade)

☛: Bug (restriction, not corrected by version upgrade)

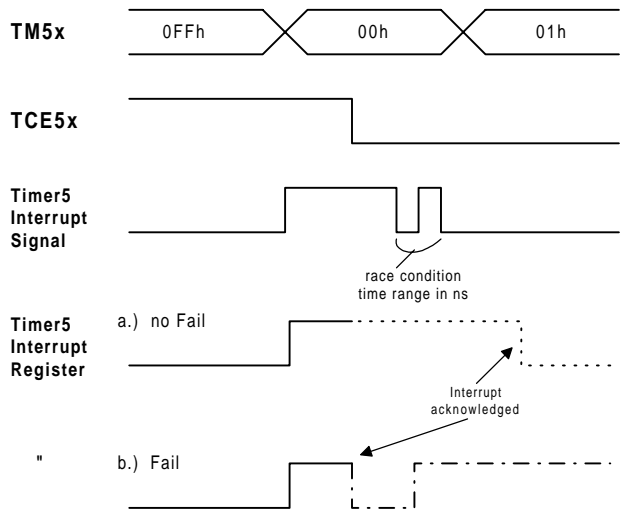
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(B) BUG DESCRIPTION

Bug No.	Outline	Description				
1	Flash memory characteristics	Details				
		These products do not satisfy the specification with respect to the number of write / erase cycles.				
			Number of W/E Times	Operating Temperature	Temperature for Rewriting	Data Retention Time
		Target spec	20 Times	-40 to + 85	0 to 40	10 years
		V1.0 ES	5 to 20 Times	-40 to +85	25	No general guarantee!
		V1.0 CS	1 Time	-40 to + 85	10 to 40	No general guarantee! A check of the application with the engineering side is necessary!
		<p>For a data retention of 10 years it is necessary to observe that VPP is 10.3V, that pre-write is disabled and that the device will be not erased.</p> <p>The following caution items apply when using the Flashpro2 (Ver. 2.1):</p> <p><1> Set erase time to 0 seconds. Select <i>erase time</i> from <i>option</i> on the <i>setting</i> command and set to 0 sec.</p> <p><2> Set pre-write to off. The pre-write set window is displayed when you press <i>ctl + shift + graph + p</i>. Click <i>OFF</i> to clear (default is <i>ON</i>).</p> <p>The following caution items apply when using the FlashMaster (Ver. 1.1 and V2.0):</p> <p><1> Set erase time to 0 seconds. Select setup from device menu and set the erase time to 0 in the advanced folder.</p> <p><2> Set pre-write to off. Select setup from device menu and disable the pre-write in the erase part of the advanced folder.</p>				

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2	A/D Converter	Details
2a		When starting the A/D conversion with the ADCS0 bit set to "1", the first A/D conversion value may be quite different from the expected value. Thus, use one of the following conversion values only!
2b		When a write operation to the A/D converter control registers (ADM0, ADMS0) appears at the same time when the A/D conversion interrupt (INTAD) is generated, the A/D conversion result register (ADCR0) becomes undefined. Therefore, a read operation from ADCR0 must be performed before a write operation to ADS0 and / or ADM0 is done.
3	VAN UDL	No detailed information.
4	Timer 5n – data match	Details
4a		In case customer use Interval timer operation mode: When Timer register (TM5n) matches with the compare register (CR5n), in the same time than the customer does a write-operation to CR5n, the agreement of the signal will be not generated.
4b		In case customer use Square-wave output operation mode: When Timer register (TM5n) matches with the compare register (CR5n), in the same time than the customer does a write-operation to CR5n, the agreement of the signal will be not generated. Further timer output F/F is not inverted.
4c		In case customer use PWM output operation mode: 1) At first the customer does a write-operation to the CR5n master register. When the customer does a rewrite-operation to the CR5n master register at the overflow timing of the timer register, a special case will be generated. The special case is that the expected data will be not transferred to the CR5n slave register. 2) When customer does a read-operation to the CR5n master register at the overflow timing of timer register, the transfer of data will be not transferred from the CR5n master register to the CR5n slave register. At the next overflow timing, the transfer of data will be operated. 3) When the timer register (TM5n) matches with the compare register (CR5n), in the same time than the customer does a write-operation to the CR5n register, the agreement of the signal will be not generated and further not be inactive level.

5	Timer 5n – interrupt	<p>The Timer5 generates a carry information in the PWM-Mode, if the counter reaches the value 0FFh. This signal is used to generate the interrupt signal. If during that time TCE5x bit is cleared a second interrupt might be generated.</p> <p>Delays in two depending paths are in a race condition. It, means, the occurrence of this bug depends on process condition and operation condition such as VDD and temperature.</p> <p><u>Typical fail behaviour:</u></p>  <p>As shown in the diagram above, the second interrupt can only occur if the interrupt is acknowledged and the TCE5x is cleared and the timer5 has the value 00h after an overrun.</p> <p>This scenario seems only feasible if the timer5x is configured with a slow pre-scaler clock and a short interrupt time.</p> <p><u>Work Around</u></p> <p>Via Software</p> <p>To be aware of this problem via software, we have only to mask the interrupt before we stop the operation of the timer5 with reset the register TCE5x.</p> <p>Please see below a few sample code lines:</p> <pre> : SET1 TMMK5x ; mask the interrupt of timer5x CLR1 TCE5x ; stop operation of timer5x CLR1 TMIF5x ; clear the interrupt register of timer5x CLR1 TMIF5x ; clear the interrupt register of timer5x CLR1 TMMK5x ; clear the mask of the interrupt of ; timer5x : </pre>
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