Concerned Products:	**Customer Notification**	Date: March 26th, 1999
		NEC-Electronics (Europe) GmbH EAD -Technical Product Support
µPD78F0034A µPD78F0034AY µPD780034A µPD780034AY µPD780033A µPD780033AY µPD780032A µPD780032AY µPD780031A µPD780031AY µPD780024A µPD780024AY µPD780023A µPD780023AY µPD780022A µPD780022AY µPD780021A µPD780021AY	**Bug Report**	Source Doc: SBB-T-10808
		Author: P. Diederichs / A. Wohlfahrt

Date of initial issue:	Nov. 9th, 98	Doc. No.:	TPS-LE-B-0031
1st edition :	Mar. 26th, 99	Doc. No.:	TPS-LE-B-0032
2nd edition :		Doc. No.:	TPS-LE-B-

(A) BUG LIST – Flash Device

Bug No.	Outline	78F0034 V3.x	78F0034Y V3.x	78F0034A **Note 1:**	78F0034AY **Note 1:**	78F0034A **Note 2:**	78F0034AY **Note 2:**		
1	Operating voltage / operating speed	✸/✸	✸/✸	✓/✓	✓/✓	✓/✓	✓/✓		
2	ESD resistance	✸	✸	✓	✓	✓	✓		
3	AD Converter	✸	✸	☺	☺	☺	☺		
4	Timer 0	✸	✸	✓	✓	✓	✓		
5	UART	✸	✸	✓	✓	✓	✓		
6	IIC Interface	no IIC	✸	no IIC	✓	no IIC	✓		
7	Flash memory characteristics	✸	✸	☟	☟	✓	✓		

✓: No problem, anymore

☺: Limitation is already improved. For details pls. refer to page 3, item 3 c

☟: Limitation will be improved in next version.

✸: Bug restriction

Note 1: Relevant devices in accordance to this list will be marked in the date code with xxxxKxxxx or xxxxExxxx

Note 2: Relevant devices in accordance to this list will be marked in the date code with xxxxPxxxx or xxxxXxxxx

(B) BUG LIST – Mask Device

Bug No.	Outline	78002x 78003x V2.0	78002xY 78003xY V2.0	78002xA 78003xA	78002xAY 78003xAY				
1	Operating voltage / operating speed	✓/✓	✓/✓	✓	✓				
2	ESD resistance	✸	✸	✓	✓				
3	AD Converter	✸	✸	☺	☺				
4	Timer 0	✸	✸	✓	✓				
5	UART	✸	✸	✓	✓				
6	IIC Interface	no IIC	✸	no IIC	✓				
7	Flash memory characteristics	no Flash	no Flash	no Flash	no Flash				

✓: No problem, anymore

☺: Limitation is already improved. For details pls. refer to page 3, item 3 c

✋: Limitation will be improved in next version.

✸: Bug restriction

(B) BUG DESCRIPTION

<table>
<tr><td>1</td><td>Operating voltage and operating speed</td><td>Details
The 78F0034 V3.x products do not satisfy the specification with respect to the operating voltage range and operating speed.
<table>
<tr><td></td><td>Supply Voltage</td><td>Operating Speed</td><td>Other</td></tr>
<tr><td>Target spec</td><td>1.8 to 5.5 V</td><td>0.24us to 32us</td><td>Subclock operation possible</td></tr>
<tr><td>V3.x</td><td>2.7 to 5.5V</td><td>0.24us to 1us</td><td>Subclock operation impossible</td></tr>
<tr><td>78F0034A</td><td>1.8 to 5.5 V</td><td>0.24us to 32us</td><td>Subclock operation possible</td></tr>
</table></td></tr>
<tr><td>2</td><td>ESD resistance</td><td>Details
The ESD resistance for the N-Ch open drain pins (P30 to P33) does not satisfy the NEC standard MIL 883D, 2kV. The current achievement is 1.1kV only.</td></tr>
<tr><td>3
3a

3b

3c</td><td>A/D Converter</td><td><u>For 78F0034 V3.x and 78F0034A:</u>
When starting the A/D conversion with the ADCS0 bit set to “1”, the first A/D conversion value may be quite different from the expected value. Thus, use one of the following conversion values only!
When a write operation to the A/D converter control registers (ADM0, ADS0) appears at the same time when the A/D conversion interrupt (INTAD) is generated, the A/D conversion result register (ADCR0) becomes undefined. Therefor, a read operation from ADCR0 must be performed before a write operation to ADS0 and /or ADM0 is done.
<u>For 78F0034 V3.x:</u>
Any difference in potential between AVREF and AVDD(=VDD) may cause the A/D conversion precision to differ from the specification.
The A/D operating voltage of these products is 2.7V to 5.5V
<u>For 78F0034A :</u>
The A/D operating voltage of these products is 2.7V to 5.5V</td></tr>
<tr><td>4
4a

4b</td><td>Timer 0</td><td>A valid edge is erroneously generated at the moment when TM0 count operation starts. This erroneous count occurs only when a rising edge is specified as a valid edge for the external event input pins TI00, TI01 and TI01 is driven high.

The timer output (TO0) will operate in reverse if TM0 is used in one-shot mode.</td></tr>
</table>

Bug No.	Outline	Description
5	UART	After receiving interrupt (INTSR), ensure a sufficient wait time (t_{READ}) before reading the receiver buffer register (RXB). The wait time should be at least one source clock cycle, which was selected by TPS00, TPS01 and TPS02 at the baud rate generator control register (BRGC0) Example: fx = 8 MHz, BRGC0 = 5AH (= 4800Bd) For this setting, pls. wait for more than 2^5 / fx = 4us
6 6a	IIC Interface	Valid for Single Master and Multi Master mode When the restart operation is used, for example: Start condition 1 -> Address 1 (write) -> Data 1 -> start condition 2 -> Address 2 (read) -> Data 2 -> Stop condition The writing of the transfer address 2 to the shift register IIC0 immediately after the second start condition trigger STT0, will result in a data output error! Means the shift register IIC0 is shifted by one bit at the same time. Workaround: After output of the start condition 2 (STT0=1), wait until the condition STT0=0 and STD0=1 becomes true. After that, write the address 2 into IIC0 register.
6b 6c		Valid for Multi Master mode If the IIC is selected as the slave during a transmit request, it returns an NAK signal instead of an ACK. The contention between the STT0 flag setting operation and start condition may cause the following bugs: a) The STT0 flag is not set b) The IIC may illegally lose the arbitration and clears STT0 during arbitration c) Setting STT0 flag may enter a transmission request state when SCL is at high level immediately after detection of a start condition.

<table>
<tr><th>Bug No.</th><th>Outline</th><th>Description</th></tr>
<tr><td>7</td><td>Flash memory characteristics</td><td>Details
These products do not satisfy the specification with respect to the number of write / erase cycles.
<table>
<tr><td></td><td>Number of W/E Times</td><td>Operating Temperature</td><td>Temperature for Rewriting</td><td>Data Retention Time</td></tr>
<tr><td>Target spec
78F0034A</td><td>20 Times</td><td>-40 to + 85</td><td>0 to 40</td><td>10 years</td></tr>
<tr><td>78F0034
V3.3 CS</td><td>Write, only
(Do not use the erase function)</td><td>-40 to +70</td><td>25</td><td>10 years, but a sequence of three program write cycles are required.</td></tr>
<tr><td>78F0034A
xxxxExxxx
xxxxKxxxx</td><td>Write, only
(Do not use the erase function)
Note 1</td><td>-40 to + 85</td><td>+10 to 40</td><td>10 years
Note 2</td></tr>
<tr><td>78F0034A
xxxxPxxxx
xxxxXxxxx</td><td>20 Times</td><td>-40 to + 85</td><td>+10 to 40</td><td>10 years
Note 3</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td></tr>
</table></td></tr>
</table>

Note 1: The Flash Memory for “E and K” mask is still under extended qualification tests, therefore for the time being the data retention time of 10 years is guaranteed under the condition for one time write.

Note 2: Vpp must be set to 10.3V +/- 0.1V

Erase time must be set to 0 sec.

Set **pre-write** to off . Pls refer also to the attachment 1.

Note 3: Vpp must be set to 10.3V +/- 0.1V

Attachment 1

Method for executing "Pre-write off" using Flashpro2:

-) Select "**Setting**" from the menu window.
Select "**Option…**" from the next window, set the " **Erase time**" to "**0 sec**" and click the **OK** button.

-) Select "**Setting**" from the menu window.
Select "**Voltage…**" from the next window, set the " Vpp " to "10.3V" and click the **OK** button.

-) Press the following keys to enter the command input state:

CTRL + SHIFT + Alt (or GRPH) **+ P**
Disable "Pre-Write set " and click on the OK button.

Remarks:
These settings are stored in the Flashpro2 so that even if the power is turned off, the settings will take effect the next time the system is started.