

## Customer Notification

# QB-78K0LX3

## In-Circuit Emulator

## Operating Precautions

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### Target devices

**78K0/LC3**

**78K0/LD3**

**78K0/LE3**

**78K0/LF3**

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QB-78K0LX3

**(A) Table of Operating Precautions**

No.	Outline	Control-code <small>Note 1</small>	QB-78K0LX3		
			B	C <small>Note 2</small>	D <small>Note 3</small>
1	TM51 wrong selection of timer clock (Technical limitation)		X	✓	✓
2	P113 read function (Technical limitation)		X	✓	✓
3	A/D converter (Technical limitation)		X	X	✓
4	Real-time counter interrupt (Technical limitation)		X	X	✓
5	Real-time counter (Technical limitation)		X	X	✓

✓ : Not applicable  
 X : Applicable

**Notes:**

1. The "control code" is the second digit from the left in the 10-digit serial number in the warranty supplied with the product you purchased (if it has not been upgraded). If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the control code.
2. Form control code "C" onwards the emulation CPU has version V1.1 (uPD78F0495 V1.1).
3. Form control code "D" onwards the emulation CPU has version V2.1 (uPD78F0495 V2.1).

**Caution: Pls. refer to and consider the Operating Precautions mentioned in the Customer Notifications of the according devices, to which this Emulator belongs to.**

**(B) Description of Operating Precautions**

No. 1	TM51 wrong selection of timer clock (Technical limitation)										
<p>[Description] If the TCL512 to TCL510 bits are set to "111" in timer clock selection register 51 (TCL51) for 8-bit timer/event counter 51 (TM51), the timer operates at <math>f_{PRS}/2^{12}</math> and not on the output signal of timer H1 as described.</p> <table border="1" data-bbox="320 512 1474 573"> <thead> <tr> <th>TCL512</th> <th>TCL511</th> <th>TCL510</th> <th>Target Device</th> <th>Emulator</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Output signal of timer H1</td> <td><math>f_{PRS}/2^{12}</math></td> </tr> </tbody> </table> <p>fPRS: Peripheral hardware clock</p> <p>[Workaround] There is no workaround.</p> <p>[Correction] This issue is corrected in products with control code C and later.</p>		TCL512	TCL511	TCL510	Target Device	Emulator	1	1	1	Output signal of timer H1	$f_{PRS}/2^{12}$
TCL512	TCL511	TCL510	Target Device	Emulator							
1	1	1	Output signal of timer H1	$f_{PRS}/2^{12}$							
No. 2	P113 read function (Technical limitation)										
<p>[Description] Inputting to the RxD6/P113 pin is possible even if the ISC3 bit of the ISC register is set to 0 (RxD6/P113 input disabled).</p> <p>[Workaround] There is no workaround.</p> <p>[Correction] This issue has been corrected in products with control code C and later, by using a device file (DF780495) V1.11 or later.</p>											
No. 3	A/D converter (Technical limitation)										
<p>[Description] The LCD controller/driver functions and 10-bit A/D converter functions are not available when <math>AV_{REF} &lt; V_{LCO}</math>. If operated under the above condition, an invalid pulse is output from the pins used by the LCD functions.</p> <p>[Workaround] There is no workaround.</p> <p>[Correction] This issue will be corrected in products with control code D and later.</p>											

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No. 4	Real-time counter interrupt (Technical limitation)
	<p>[Description] When a fixed-cycle interrupt and an alarm interrupt occur at the same time, the WAFG flag is set after one cycle of the clock input to the real-time counter.</p> <p>[Workaround] When an INTRTC interrupt occurs, check the RIFG flag first. If the RIFG flag has been set to "1", wait for one cycle of the clock input to the real-time counter and then check the WAFG flag again.</p> <p>[Correction] This issue will be corrected in products with control code D and later.</p>
No. 5	Real-time counter (Technical limitation)
	<p>[Description] If the real-time counter (RTC) is stopped when the count value of the sub-count register (RSUBC) reaches 7FFDH or 7FFEh, the RTCE bit is cleared to "0" but the second count register (SEC) may not stop and continues to count up at the real-time counter input clock cycles.</p> <p>[Workaround] Before stopping the RTC, first set the RWAIT bit and then confirm that the RWST flag has set to "1".</p> <p>[Correction] This issue will be corrected in products with control code D and later.</p>

**(C) Valid Specification**

<b>Item</b>	<b>Date published</b>	<b>Document No.</b>	<b>Document Title</b>
1	December, 2006 or later	U18511EJ	User's Manual

**(D) Revision History**

<b>Item</b>	<b>Date published</b>	<b>Document No.</b>	<b>Comment</b>
1	December 2007	TPS-LE-OP-TQBLX3-1	1 <sup>st</sup> Release
2	January 2008	TPS-LE-OP-TQBLX3-2	1 <sup>st</sup> Update, addition of items 2-5