NEC

Customer Notification

QB-70F3469

In-Circuit-Emulator

Operating Precautions

Target Device

µPD70F3469

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(A) Product Version

1. Product Code:

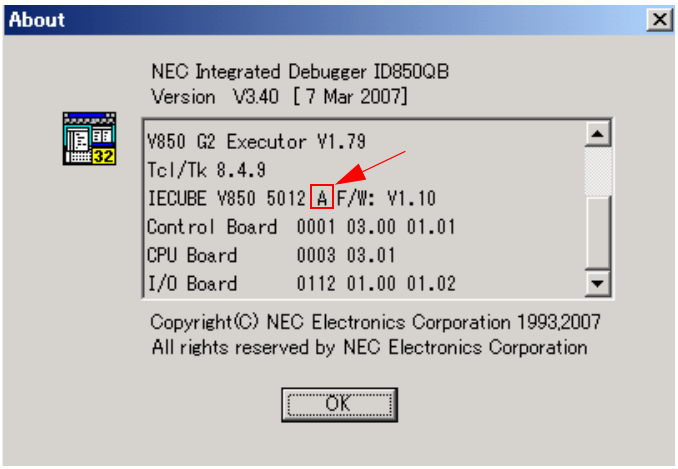
Control Code[Note]	Remarks
A	-

Note: The “control code” is the second digit from the left in the 10-digit serial number printed on the sticker attached to the bottom side of IECUBE (if it has not been upgraded). If the product has been upgraded, the control code can also be checked with the following methods while the debugger is running.

•When using ID850QB

Click the [Help] menu and then click the About submenu to display the About dialog box.“X” in “IECUBE V850 **** X F/W: V*.**” is the control code

.



•When using Green Hills Software (GHS)’s debugger MULTI

Execute the version command of 850eserv.

“X” in “IECUBE Control Code=X” is the control code.

```
850eserv Version: 3.2342 (for MULTI V4.0.x)
IE type=NU85E Full ICE Generation 2 (IECUBE)
Executor Version=V850 G2 Executor V1.63
Copyright 2004
Device File Format Version=V2.18
Device File File Version=V2.10
IECUBE Control Code=A
IECUBE Firmware Version=V1.10
Control Board Version=V2.02 (FPGA
Version=0.01)
CPU Board Version=V3.00
I/O Board Version=V1.01 (FPGA Version=0.01)
```

(B) Table of Operating Precautions

No.	Outline	ControlCode	QB-70F3469
			A
1	Access to CnRGPT register during break (n = 0 to 3) (Specification change notice)		✗
2	Access to CnTGPT register during break (n = 0 to 3) (Specification change notice)		✗
3	Access to CnGNCTRL register during break (n = 0 to 3) (Specification change notice)		✗
4	Program execution and DMA transfer in internal RAM (Direction of use)		✗
5	Emulation of POC circuit and clock monitor (Direction of use)		✗
6	Break during program execution in internal RAM (1) (Specification change notice)		✗
7	Reset input during a break (Direction of use)		✗
8	Entering and releasing STOP mode when $\overline{\text{RESET}}$ pin is masked (Specification change notice)		✗
9	Break occurs during program execution in internal RAM (2) (Specification change notice)		✗
10	Accessing CBnRX register during break (n = 0 to 2) (Specification change notice)		✗

✓ Not applicable
✗ Applicable

(C) Description of Operating Precautions

No. 1	Access to CnRGPT register during break (n = 0 to 3) (Specification change notice)

Details

Under the following conditions (a) and (b), the read pointer (RGPT) that should be incremented is not incremented, and the same data as previously read is read.

(a) If a software break occurs immediately after reading the CANn module receive history list register (CnRGPT).

(b) If a DMA transfer from the CANn module receive history list register (CnRGPT) is performed during a break[NOTE].

Note: Including breaks by the RAM monitor function, DMM function, step-wise execution, fail-safe break, or breaks due to event change while the program is running. The real-time RAM monitor function does not cause this behaviour because it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CnRGPT register.

(b) There is no workaround.

No. 2	Access to CnTGPT register during break (n = 0 to 3) (Specification change notice)

Details

Under the following conditions (a) and (b), the read pointer (TGPT) that should be incremented is not incremented, and the same data as previously transmitted is transmitted.

(a) If a software break occurs immediately after reading the CANn module transmit history list register (CnTGPT).

(b) If a DMA transfer from the CANn module transmit history list register (CnTGPT) is performed during a break[Note].

Note: Including breaks by the RAM monitor function, DMM function, step-wise execution, fail-safe break, or breaks due to event change while the program is running. The real-time RAM monitor function does not cause this behavior because it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CnTGPT register.

(b) There is no workaround.

No. 3	Access to CnGMCTRL register during break (n = 0 to 3) (Specification change notice)

Details

When a register access is performed in the following sequence, a forcible shutdown that should not take place normally may occur after the sequence is complete.

Sequence:

(1) The EFSD bit of the CANn module control register (CnGMCTRL) is set.

(2) The I/O register[Note] is accessed.

(3) The GOM bit of the CANn module control register (CnGMCTRL) is cleared.

Note: I/O register access except for clearing the GOM bit of the CnGMCTRL register

Conditions under which a forcible shutdown takes place are shown below:

(a) If a break occurs immediately after the I/O register access in (2) occurs

(b) If a break by the RAM monitor function or DMM function occurs immediately after the I/O register access in (2) occurs

(c) Stepwise execution is performed for the I/O register access in (2)

Workaround

Be sure to set the EFSD bit and clear the GOM bit successively when executing a forcible shutdown. Do not perform register access in the above sequence when not performing a forcible shutdown.

No. 4	Program execution and DMA transfer in internal RAM (Direction of use)

Details

When a data access instruction for a misaligned address allocated in the internal RAM and DMA transfer for the internal RAM are executed simultaneously, the CPU may deadlock due to conflict between the internal bus operations. At this time, only a reset can be acknowledged, an NMI or interrupt cannot be acknowledged.

Unaffected cases

The critical situation does not occur if no instruction is executed in the internal RAM, or no DMA transfer is performed on the internal RAM.

Workaround

Implement either of the following workarounds.

(1) Do not perform a DMA transfer for the internal RAM when a data access instruction for a misaligned address allocated in the internal RAM is being executed.

(2) Do not execute a data access instruction for a misaligned address allocated in the internal RAM when a DMA transfer for the internal RAM is being performed.

No. 5	Emulation of POC circuit and clock monitor (Direction of use)

Details

The POC circuit and the clock monitor cannot be emulated.

Workaround

There is no workaround.

No. 6	Break during program execution in internal RAM (1) (Specification change notice)

Details

An expected break may occur when a peripheral I/O register is accessed during program execution in the internal RAM.

Workaround

Cancel the fail-safe break setting for the internal RAM in the debugger.

- When using ID850QB
  Select Configuration/Fail-save Break/Detail and clear the check box for 'Internal RAM'.
- When using MULTI
  Cancel the fail-safe break for "ramgrd" and "ramgrdv" using the Target command "flsf".

No. 7	Reset input during a break (Direction of use)

Details

The QB-70F3469 may hang up if a break occurs when the RESET pin is active (low level).

Workaround

Mask the RESET pin using the pin mask function of the debugger.

No. 8	Entering and releasing STOP mode when RESET pin is masked (Specification change notice)

Details

When the RESET pin is masked using the pin mask function of the debugger and watchdog timer 2 is used in reset mode, the CPU's operating clock is switched to internal oscillation clock after STOP mode is released, depending on the timing for entering and releasing STOP mode (one of the cases (1)to (3) in the following table).
After the clock is switched to internal oscillation clock, the CPU continues the operation with internal oscillation clock until the CPU reset function of the debugger is pressed.

No.	Operating Clock for Watchdog Timer 2	Conditions
(1)	Main clock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released[Note]
(3)	Internal oscillation clock	STOP mode is entered during the period from when a reset of watchdog timer 2 occurs until the reset is released[Note]
(4)		The internal oscillation clock is stopped during the period from when a reset of watchdog timer 2 occurs until the reset is released[Note], and then STOP mode is entered

Note: The period in which watchdog timer 2 generates a reset signal while the reset signal of watchdogtimer 2 is masked as a result of masking RESET using the pin mask function of the debugger.

Workaround

Implement either of the following workarounds.

- To prevent a reset of watchdog timer 2 from occurring, stop watchdog timer 2 by using software before the reset occurs.
- To generate a reset of watchdog timer 2, do not mask the RESET pin using the pin mask function of the debugger.

No. 9	Illegal break occurs during program execution in internal RAM (2) (Specification change notice)

Details

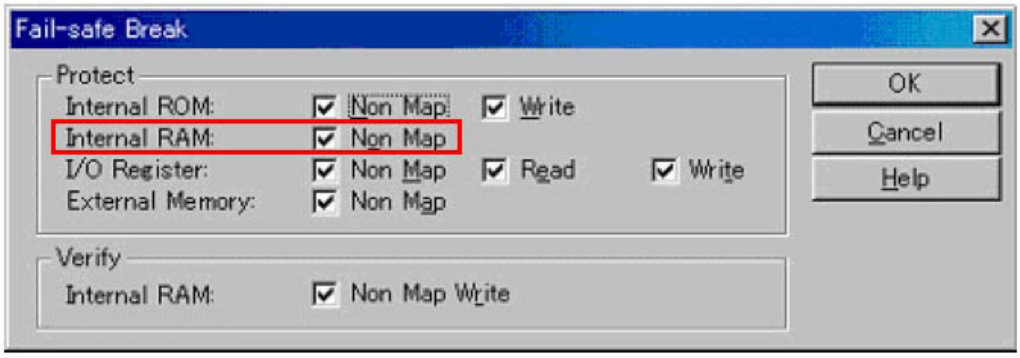
A non-map break occurs if all of the following conditions are satisfied, even if the program itself is correct.

- A program is executed in the internal RAM area.
- Data access for the internal RAM area is performed twice in succession.
- An execution branches to the internal ROM area using a JR or JARL instruction immediately after the above successive data access, or one NOP instruction after the above successive data access.

Workaround

Implement either of the following workarounds.

- Cancel the fail-safe break setting for the internal RAM in the debugger.
  - When using ID850QB
    Select Configuration/Fail-save Break/Detail and clear the check box 'Non Map' for 'Internal RAM'.



  - When using MULTI
    Cancel the fail-save break for 'ramgrd' and 'ramgrdv' unsing the Target command 'flsf'.
- Insert two or more NOP instructions between the successive data access for the internal RAM area and an instruction to branch to the internal ROM area.

No. 10	Accessing CBnRX register during break (n = 0 to 2) (Specification change notice)

Details

When the CSIBn receive data register (CBnRX) is read, the next reception operation starts in the normal operation. Under the following conditions (a) and (b), however, the next reception operation is not started even if CBnRX is read. As a result the communication stops or the DMA controller stops.

(a) If a software break occurs immediately after reading the CSIBn receive data register (CBnRX).

(b) If a DMA transfer from the CSIBn receive data register (CBnRX) is performed during a break**Note**.

Note: Including breaks by the RAM monitor function, DMM function, step-wise execution, fail-safe break, or breaks due to event change while the program is running. The real-time RAM monitor function does not cause this behaviour because it does not set breaks.

Workaround

(a) Set a hardware break when setting a break immediately after reading the CBnRX register.

(b) There is no workaround.

(D) Valid Specification

Item	Date pulished	Document No.	Document Title
1	December 2007	ZUD-CD-07-0219	QB-70F3469 User's Manual

(E) Revision History

Item	Date pulished	Document No.	Comment
1	October, 2008	U19499EE1V0IF00	First release.