NEC

Customer Notification

QB-703426

In-Circuit-Emulator

Operating Precautions

Target Device - V850E/Dx3

uPD70(F)3424/425/426™

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(A) Table of Operating Precautions

No.	Outline		QB-703426			
		Ctrl.-Code	A			
		Date	08.06.06	07.04.08		
		Version IO	V1.20-1.40 V2.00-2.10	V1.20-1.40 V2.00-2.10		
		Version FPGA IO	V4.02	V4.05		
		Version VM	V1.01	V1.01		
		Version FPGA VM	V1.00	V1.00		
1	Internal On-chip oscillator frequency is fixed to 200 kHz (Technical limitation)		Y	Y		
2	Fout- and WDT-clock supply differ from device in stand by mode (Specification change notice)		Y	Y		
3	PSM.OSCDIS reset value different to device (Specification change notice)		Y	Y		
4	Timing different to device for oscillation stabilisation time (Specification change notice)		Y	Y		
5	Break precaution related to ADC macro (Specification change notice)		Y	Y		
6	Open-Drain Port mode not implemented (Technical limitation)		Y	N		

N : Not applicable

Y : Applicable

Note: The control code is the second letter from the left of the 10 digit serial number or in case of update the latest control code is mentioned on the version up sticker.

(B) Description of Operating Precautions

No. 1	Internal On-chip oscillator frequency is fixed to 200 kHz
	Details: The internal On-chip oscillator frequency may differ from the device version to be emulated. *Workaround:* None

No. 2	Fout- and WDT-clock supply differ from device in stand by mode
	Details: In stand by mode, the FOUT clock supply (Internal On-chip oscillator clock, if ROSTP=1 is set) will not stop. In stand by mode, the FOUT clock supply (Sub-clock, if SOSTP=1 is set) will not stop. In stand by mode, the WDT clock supply (Internal On-chip oscillator clock, if ROSTP=1 is set) will not stop. In stand by mode, the WDT clock supply (Sub-clock, if SOSTP=1 is set) will not stop. *Workaround:* None.

No. 3	PSM.OSCDIS reset value different to device
	Details: The reset value of the OSCDIS is ‘1’. On real chip OSCDIS is set to ‘0’ during firmware execution. *Workaround:* Initialise the OSCDIS after RESET or use the functions of the Debugger to initialize the OSCDIS before program start.

No. 4	Timing different to device for oscillation stabilization time
	Details: The oscillation stabilization time indicated by OSCSTAT differ to real device. In emulation mode the oscillator run permanently, so the time for oscillation start is not given. After reset, out of the different OSCDIS setting, the oscillation stabilization counter start is different. *Workaround:* None

No. 5	Break precaution related to ADC macro

Details: [Explanation]

The following Behaviour is valid for the IECUBE emulator "only" in case the peripheral break mode is active for the ADC macro:

1.) In case the peripheral break signal (SVSTOP = 1) is set while or after the conversion control bit ADA0CE has been set, the AD conversion is not started and the concerned interrupt INTAD will not be generated. Furthermore the AD conversion will not start conversion even in case the Supervisor mode has been left and the debugger operates in RUN mode.

In case the ADA0CE bit will be set during normal RUN mode again without issuing the peripheral break signal, the ADC will operate as specified.

The conditions the peripheral break signal is issued are as follows:

a.) - When one of these break is executed on the AD0ACE bit write instruction
- Software break
- Before-execution hardware break
- After-execution hardware break

b.) - When one of these break is executed on the first instruction following the AD0ACE bit write instruction
- Software break
- Before-execution hardware break

c.) - When the following break is executed on the second instruction following the AD0ACE bit write instruction
- Software break

2.) In case the peripheral break mode (SVSTOP=1) has been configured and the debugger operates in the debug (supervisor-) mode, a write operation to the ADC concerned registers:

ADA0M0, (ADA0M1(#)), ADA0M2, ADA0S, ADA0PFT, ADAPFM (#) when ADA0CE=1, the re-write of ADA0M1 is prohibited and will not cause the start of the ADC's reconversion.

It doesn't make a difference if the concerned write operations to the above mentioned ADC registers are executed via the debugger itself or via DMA that is not stopped when entering the supervisor mode. Both write operations will cause the limitation.

No. 5	Break precaution related to ADC macro (2nd page)

Workaround: [Restrictions]

a) When a software break is executed in case the peripheral break mode has been configured for the ADC macro, set the software break not for the instruction the ADA0CE bit is set or at one of the following two instructions:

Example:

```
set1 7, ADA0M0   --- software break is prohibited
nop              --- software break is prohibited
nop              --- software break is prohibited
nop              --- software break is possible to set from here on
```

b) When a "before-execution hardware break" is executed and the peripheral break mode has been configured for the ADC macro, don't set that breakpoint for the instruction that sets the ADA0CE bit or for the following instruction:

Example:

```
set1 7, ADA0M0   --- before-execution hardware break is prohibited
nop              --- before-execution hardware break is prohibited
nop              --- before-execution hardware break is possible to set from here on
```

c) When a "before-execution hardware break" is executed in peripheral break mode and the peripheral break mode has been configured for the ADC macro, don't set that breakpoint for the instruction that sets the ADA0CE bit:

Example:

```
set1 7, ADA0M0    --- after-execution hardware break is prohibited
nop               --- after-execution hardware break is possible to set from here on
```

d) When users want to proceed the write operation for the AD related registers during BREAK (debugger operates within the supervisor mode), don't use peripheral break mode.

e) When users want to proceed the DMA transfer which has AD related registers set as source/destination for this DMA transfer <<<, don't use peripheral break mode.

Note: In case a condition mentioned under "Workarounds: a), b), c)" will occur when setting one of the concerned breakpoints on the location of an interrupt-vector, no limitation will become valid due to the clock-cycles that are requested for the interrupt-response time!

No. 6	Open-Drain Port mode not implemented
	Details: The register access (read/write) of PODCx is possible, but the function itself isn't supported. The following Port is affected: P0[7]. *Workaround:* None

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	April 2008	EEDT-OP-0033-5.0	This document
2	April 2007	U18352EE1V0UM00	Preliminary User's Manual QB-703426
3	April 2007	U18350EE1V0UM00	Preliminary User's Manual QB-703427

(D) Revision History

Item	Date published	Document No.	Comment
1	June 2006	EEDT-OP-0033-1.0	1st release
2	April 2007	EEDT-OP-0033-2.0	1st update (new UM)
3	July 2007	EEDT-OP-0033-3.0	2nd update (Text correction)
4	November 2007	EEDT-OP-0033-4.0	3rd update (New item No. 6)
5	April 2008	EEDT-OP-0033-5.0	4th update (Update item No. 6)