NEC

Customer Notification

78K0/Kx1 Series™

8-Bit Single-Chip Microcontrollers

Operating Precautions

78K0/KB1:
µPD780101, µPD780102,µPD780103, µPD78F0103Mx
78K0/KC1:
µPD780111, µPD780112,µPD780113, µPD780114
µPD78F0114Mx
78K0/KD1:
µPD780121, µPD780122,µPD780123, µPD780124
µPD78F0124Mx
78K0/KE1:
µPD780131, µPD780132,µPD780133, µPD780134 µPD780136,
µPD780138, µPD78F0134Mx, µPD78F0138Mx
78K0/KF1:
µPD780143,µPD780144,µPD780146,µPD780148,µPD78F0148Mx

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78K0/Kx1 Series

Mask ROM versions

		Description	78K0/KB1 µPD780101 µPD780102 µPD780103	78K0/KC1 µPD780111 µPD780112 µPD780113 µPD780114		78K0/KD1 µPD780121 µPD780122 µPD780123 µPD780124		78K0/KE1 µPD780131 µPD780132 µPD780133 µPD780134 µPD780136 µPD780138		78K0/KF1 µPD780143 µPD780144 µPD780146 µPD780148	
		Rank [Note]	K	K	E	K	E	K	E	K	E
		Version	-	-	-	-	-	-	-	-	-
1	Restriction on writing to flash memory (technical limitation)		-	-	-	-	-	-	-	-	-
2	Restriction in detection voltage in POC and LVI (technical limitation)		-	-	-	-	-	-	-	-	-
3	Restriction on POC (technical limitation)		-	-	-	-	-	-	-	-	-
4	Restriction on clock monitor (technical limitation)		-	-	-	-	-	-	-	-	-
5	Restriction on automatic transfer 3-wire CSI (technical limitation)		-	-	-	-	-	-	-	-	-
6	Restriction on SBF transmission using UART6 (direction of use)		✗	✗	✗	✗	✗	✗	✗	✗	✗
7	Restriction on16-bit timer output (direction of use)		✗	✗	✗	✗	✗	✗	✗	✗	✗
8	Restriction on connection when XT1 is not used (technical limitation)		-	✗	✓	✗	✓	✗	✓	✗	✓
9	Restriction on oscillation stabilization time (direction of use)			✗	✗	✗	✗	✗	✗	✗	✗

Flash memory version

		Description	78K0/KB1 μPD78F0103				78K0/KC1 μPD78F0114		78K0/KD1 μPD78F0124		78K0/KE1 μPD78F0134 μPD78F0138		78K0/KF1 μPD78F0148				
		Rank[Note]	I			K	K	E	K	E	K	E	I			K	E
		Version	1.0	1.1 - 2.2	2.2	-	-	-	-	-	-	-	1.1	2.0	2.1	-	-
1	Restriction on writing to flash memory (technical limitation)		✗	✓	✓	✓	-	-	-	-	-	-	-	-	-	-	-
2	Restriction in detection voltage in POC and LVI (technical limitation)		✗	✓	✓	✓	-	-	-	-	-	-	-	-	-	-	-
3	Restriction on POC (technical limitation)		✗	✓	✓	✓	-	-	-	-	-	-	-	-	-	-	-
4	Restriction on clock monitor (technical limitation)		✗	✗	✓	✓	-	-	-	-	-	-	-	-	-	-	-
5	Restriction on automatic transfer 3-wire CSI (technical limitation)		-	-	-	-	-	-	-	-	-	-	✗	✗	✓	✓	✓
6	Restriction on SBF transmission using UART6 (direction of use)		✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
7	Restriction on16-bit timer output (direction of use)		✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗
8	Restriction on connection when XT1 is not used (technical limitation)		-	-	-	-	✗	✓	✗	✓	✗	✓	✗	✗	✗	✗	✓
9	Restriction on oscillation stabilization time (direction of use)		✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗	✗

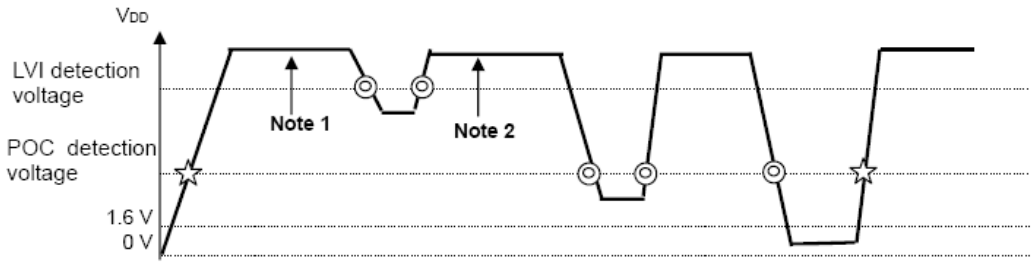
✓: Not applicable
✗: applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(A) Description of Operating Precautions

No. 1	UART 6 Restriction on writing to flash memory (technical limitation)
	Details UART6 cannot be used in flash memory writing communication mode. Writing to the flash memory cannot be performed when UART6 is used in flash memory writing communication mode. Do not use UART6 for flash memory writing, use the 3-wire serial I/O or UART0 instead.

No. 2	Restriction in detection voltage in POC and LVI (technical limitation)
	Details The voltage detected by the power-on-clear circuit (POC) and low-voltage detector (LVI) is 0.1 to 0.3 V (TYP.) lower than that of the specification.

No. 3	Restriction on POC (technical limitation)
	Details A reset using POC may not be possible immediately after power application. Therefore, an external reset should be used immediately after power application. A reset using POC at the fall of the power supply and when the voltage is raised from the POC detection voltage > V_{DD} > 1.6 V can be generated normally. In addition, a reset is also generated normally at the rise/fall of the power supply when using LVI with a voltage higher than the POC detection voltage.  ☆: RESET cannot be applied normally. Apply an external RESET. ◎: RESET can be applied normally. **Note 1**: LVI is set to RESET by software (LVIMD ← 1) **Note 2**: LVI operation stopped or is set to interrupt by software (LVION ← 0 or LVIMD ← 0)

No. 4	Restriction on clock monitor (technical limitation)

Details

The operation status of CLM (clock monitor mode register) can be manipulated even after the clock monitor operation is set.

Once bit 0 of CLM (clock monitor mode register) is set (1), the clock monitor cannot be cleared using a method other than RESET input or internal reset signal. However, operation of the clock monitor can actually be set by manipulating CLM by a software instruction.

Do not clear bit 0 of the CLM register once it is set (1); otherwise the clock monitor stops.

Bit 0 of CLM Register	Clock Monitor Operation
0	Stops
1	Operates

No. 5	Restriction on automatic transfer 3-wire CSI (technical limitation)

Details

When writing transmit data to the buffer RAM using the 3-wire serial interface with automatic transfer function (CSIA0), data may not be written correctly depending on the instruction executed after the write instruction.

This restriction is not applicable under the following condition:

Condition: CSIA0 input clock (fSCKA) is faster than the CPU operating clock (fcpu) x 10

$$fcpu \times 10 < fSCKA \qquad (fSCKA: CSIA0 \text{ input clock} = fx)$$

This condition is only applicable when:

fx is selected as the CSIA0 operating clock, and $fx/2^4$
or
fxt is selected as the CPU operating clock (when the main clock is oscillating) in the 78K0/KF1.

Workarounds

1. Interrupts are not disabled when writing to the buffer RAM

Write data to the buffer RAM using the 16-bit data transfer instruction only, and then read back the data to compare with the written value. If the data do not match, write the same value again. At this time, it is not necessary to disable interrupts.

When writing an odd number of bytes (if it is needed to write data to the even address), write dummy data to the buffer RAM at the higher address of the last address.

```
Example:    BRAMW1:   MOVW AX,#0AA55H
                      MOVW !0FA00H,AX     ; Buffer RAM write instruction
                      MOVW AX,!0FA00H
                      CMPW AX,#0AA55H     ; Comparison with expected data
                      BF PSW.6,$BRAMW1
                ;
                BRAMW2:   MOVW AX,#5A69H
                      MOVW !0FA02H,AX     ; Buffer RAM write instruction
                            :
```

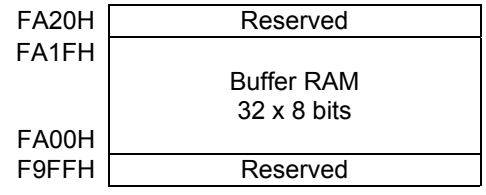


Figure: Buffer RAM Configuration

2. When interrupts are disabled when writing to the buffer RAM (using the 16-bit data transfer instruction)

Disable interrupts using the DI instruction and write data to the buffer RAM using the 16-bit data transfer instruction only. In addition, rewrite the last 2 bytes of the written data again. Do not execute instructions other than NOP and operation instructions between data are written to the buffer RAM and the last 2 bytes are rewritten.

Example:

```
DI                  ; Disables interrupt
MOVW AX,#0AA55H
MOVW !0FA00H,AX     ; Buffer RAM write instruction
MOVW AX,#5A69H
MOVW !0FA02H,AX     ; Buffer RAM write instruction
      :
MOVW AX,#1234H
MOVW !0FA1EH,AX     ; Buffer RAM write instruction (last
                    ; address)
MOVW !0FA1EH,AX     ; Rewrite
EI                  ; Enables interrupt
```

3. When interrupts are disabled when writing to the buffer RAM (using the 8-bit data transfer instruction)

Disable interrupts using the DI instruction and write data to the buffer RAM using the 8-bit data transfer instruction only. In addition, execute a NOP instruction or operation instruction after the last data is written to the buffer RAM.

Example:

```
DI                  ; Disables interrupt
MOV A,#0AAH
MOV !0FA00H,A       ; Buffer RAM write instruction
MOV A,#055H
MOV !0FA01H,A       ; Buffer RAM write instruction
      :
MOV A,#12H
MOV !0FA1FH,A       ; Buffer RAM write instruction (last
                    ; address)
NOP
EI                  ; Enables interrupt
```

No. 6	Restriction on SBF transmission using UART6 (direction of use)

Details

Thids limitation occurs when using UART 6 in LIN master mode. The limitation is encountered when sending a SyncBreakField. The following events may occure:

1. Unexpected length of SyncBreakField

Using the special implementation to send the SyncBreakField by setting the SBTT6-Bit in the ASICL6-Register, it may occur that the SyncBreakField will be send with a length of one bit less than the setting in the ASICL6-Register implies.

2. Illegal data in advance of SyncBreakField

Depending on internal timings, illegal data might be sent preceeding the SyncBreakField.

For detailed description and workaround, pls. refer to the document EACT-BR-5500.pdf.

No. 7	Restriction on16-bit timer output (direction of use)

Details

When setting the timer output F/F status using 16-Bit timer/event counter 00, the setting may not be performed correctly depending on the timer output control register TOC00 setting timing. If LVS00 is set to 1 before setting TOE00, the LVS00 settings are invalid and a low level is output. If LVS00 and TOE00 are set to 1 simultaneously, the timer output is undefined.

Symbol	7	6	5	4	3	2	1	0
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

LVS00	LVR00	Setting of timer output F/F
0	0	No change
0	1	Timer output F/F is reset (0)
1	0	Timer output F/F is set (1)
1	1	Setting Prohibited

TOE00	Timer output control
0	Output disabled
1	Output enabled

Workaround

At first set TOE00 to 1 to enable timer output and then set LVS00 to 1 to output a high level from the timer.

Program example:

```
MOV   TOC00,#00000001B    ;16-Bit timer output enabled
MOV   TOC00,#00011011B    ;Other settings and timer output F/F are set to high level
                          ;(Timer output level is set to high level)
  :

MOV   TMC00,#00001100B    ;Timer operation started
```

No. 8	Restriction on connection when XT1 is not used (technical limitation)

Details

When the unused XT1 pin is connected under the following condition, the operating current increases by approx. 5 mA.

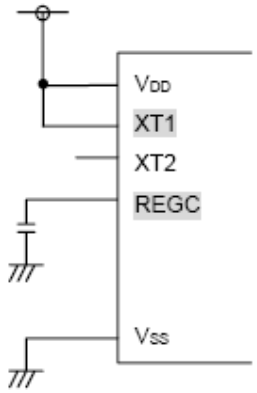
Condition: The regulator is used (the REGC pin is connected to V_{SS} vis a 1 ⌈F capacitor) and the XT1
pin is connected to V_{DD}.

This restriction does not apply if the regulator is not used (the REGC pin is connected to V_{DD}) or if the XT1 and XT2 pins are connected to the subclock.

Table 1. Relationship Between connection of XT1 and REGC Pins and Restriction

	Regulator Is Not Used (REGC Pin Is Connected to V_{DD})	Regulator Is Used (REGC Pin Is Connected to V_{SS} via 1 μF Capacitor)
Subclock is used (A 32.768 kHz resonator is connected to XT1, XT2)	Not affected by restriction.	Not affected by restriction.
Subclock is not used (XT1 is connected to V_{DD} and XT2 is left open)	Not affected by restriction.	The operating current increases by approx. 5 mA.

Figure 1. Connection of REGC and XT1 Pins That Increases Operating Current



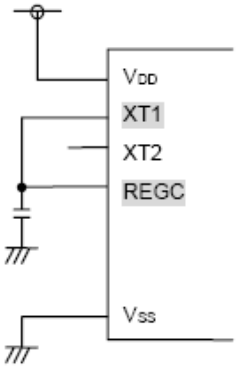
Workaround

When the regulator is used and the XT1 pin is not used, implement any of the following temporary workarounds.

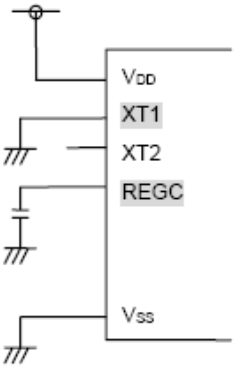
- Connect the XT1 pin to the REGC pin directly.
- Connect the XT1 pin to V_{SS}. With this workaround, however, the operating current increases by several μA.

Figure 2. Circuit Diagram When Temporary Workaround Is Implemented

(1) XT1 pin is connected to REGC pin



(2) XT1 pin is connected to Vss



Workaround

Connect the XT1 pin to GND when it is not used. In addition, the device will be modified to suppress the several ⌠A current increase.

Cautions on device modification

1. Users are not required to change software in line with this device modification.
2. The electrical specifications will not be affected by this device modification.
3. Users can use the modified device without modifying circuits or software if the regulator is not used or the subclock is connected.
4. This restriction does not apply to the 78K0/KC1, but the device will be modified so that the XT1 pin can be connected to VSS.
5. The device name will be changed after modification.
6. After this modification, the rank of the product will be E (products not modified are rank K or I).The rank is indicated by the fifth character from the left in the lot number marked on the third line on the package (see the figure below).

The relationship between the connection of the XT1 pin when it is not used, the temporary workaround, and the permanent workaround is shown in Table 2.

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Table 2. Relationship Between Connection of XT1 Pin When It Is Not Used, Temporary Workaround, and Permanent Workaround

Connection of XT1 Pin When It Is Not Used		KD1, KE1, KF1 Before Modification	KD1, KE1, KF1 After Modification	78K0/Kx1+[Note]
Current connection	Connect XT1 pin to V_{DD} (when regulator is not used, REGC pin is connected to V_{DD})	Not affected by restriction.	Not affected by restriction.	Not affected by restriction.
	Connect XT1 pin to V_{DD} (when regulator is used, a 1 μF capacitor is connected to REGC pin)	The operating current increases by approx. 5 mA.	The operating current increases by approx. 5 mA.	Not affected by restriction.
Temporary workaround	Connect XT1 pin to REGC pin (when regulator is used, a 1 μF capacitor is connected to REGC pin)	Not affected by restriction.	Not affected by restriction.	Leave the REGC pin open; otherwise a through current may flow in the XT1 and XT2 pins.
Permanent workaround	Connect XT1 pin to V_{SS} (when regulator is not used, REGC pin is connected to V_{DD})	The operating current increases by several μA.	Not affected by restriction.	Not affected by restriction.
	Connect XT1 pin to V_{SS} (when regulator is used, a 1 μF capacitor is connected to REGC pin)	The operating current increases by several μA.	Not affected by restriction.	Not affected by restriction.

Note The 78K0/Kx1+ is a 78K0/Kx1-compatible microcontroller currently under development.

No. 9	Restriction on oscillation stabilization time (direction of use)

Details

When the OSTS register (oscillation stabilization time select register) is used with a specific setting other than the initial value and the main clock oscillation stabilization time is checked using the OSTC register (oscillation stabilization time counter status register), the correct value may not be read.

Condition

OSTC Operating Status	OSTS Value Setting	OSTS Value Change Pattern (OSTS Initial Value = 05H)	Whether or Not This Restriction Is Applicable
Count status after reset or standby release	OSTS value is not set (Initial value is used)	–	Not applicable
	OSTS value is set	05H (101) → 05H (101)	Not applicable
		05H (101) → 04H (100)	Not applicable
		05H (101) → 03H (011)	Applicable
		05H (101) → 02H (010)	Applicable
		05H (101) → 01H (001)	Not applicable
		Consult NEC Electronics in regards to change patterns other than above.	–
Other than above	–	–	Not applicable

Workaround

Do not use the OSTS register under the condition to which this restriction applies.
When using the OSTS register under the condition to which this restriction applies, check the oscillation stabilization time using the OSTC register before setting the OSTS register.

(B) Valid Specification

Item	Date published	Document No.	Document Title
1	Feb 2005 or later	U15836EJ	78K0/KB1 User's Manual
2	Feb 2005 or later	U16227E	78K0/KC1 User's Manual
3	Nov 2003 or later	U16315E	78K0/KD1 User's Manual
4	July 2005 or later	U16228E	78K0/KE1 User's Manual
5	June 2005 or later	U15947E	78K0/KF1 User's Manual

(C) Revision History

Item	Date published	Document No.	Comment
1	August, 2005	TPS-LE-OP-Kx1-1	1st Release of merged version of all Kx1 products