NEC

Customer Notification

IE-703107-MC-EM1™

In-circuit Emulator Option Board

Operating Precautions

Document No. IE-703107-TPS-HE-B-2774
Date Published: June 2004

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Table of Contents

(A) Table of Operating Precautions

No.	Outline		IE-703107-MC-EM1				
		Contr Code	A	B	C	D	E
		Rank	ES1.00	ES2.00	P	P	P
1	Operating frequency restriction		✗	✓	✓	✓	✓
2	Clock direct mode restriction		✗	✓	✓	✓	✓
3	IORD, IOWR signal restriction Note1		✗	✗	✗	✗	✗
4	SFR restriction Note1		✗	✗	✗	✗	✗
5	A/D converter restriction		✗	✓	✓	✓	✓
6	Pin status restriction single chip mode 1 and ROM-less mode 0/1		✗	✓	✓	✓	✓
7	DMA start by built-in peripheral I/O interrupt Note2		✗	✗	✗	✗	✗
8	DTOC read access		✗	✗	✓	✓	✓
9	SDRAM lead access Note2		✗	✗	✗	✗	✗
10	External Interrupt		✗	✓	✓	✓	✓
11	Restriction UART		✗	✓	✓	✓	✓
12	Illegal write access to interrupt control register Note3		✗	✗	✗	✗	✗
13	A/D converter timer 1 trigger mode		✗	✗	✗	✓	✓
14	HLDAK signal output		✗	✗	✗	✗	✓

✓ : Not applicable
✗ : applicable

Note1 This restriction applies when using the IE-V850E-MC-A. This restriction is not applicable to versions with control code D or later, of IE-V850E-MC-A.

Note2 This restriction applies when using the IE-V850E-MC-A. This restriction is not applicable to versions with control code F or later, of IE-V850E-MC-A.

Note3 This restriction does not apply in combination of the IE-V850E-MC-A with control code G or later and IE-703007-MC-EM1 with control code D or later.

(B) Description of Operating Precautions

No.1	Operating frequency restriction

Details

The maximum operating frequency is 40MHz.

The restriction applies also on the IE-V850E-MC-A with control code B, C, which is limited to 40 MHz

Workaround

None.

The control code B product has been corrected so that it can operate at 50 MHz.

Please take care that this restriction applies also on the IE-V850E-MC-A with control code B, C, it is limited to 40 MHz.

No.2	Clock direct mode restriction

Details

The emulator operates at 1/2 the input clock when direct mode is selected for clock operation mode.

Workaround

None

No.3	IORD, IOWR signal restriction

Details

1. IORD and IOWR pin assignment is reversed.

V850E/MA1 pin 102: PCS5/_CS5/_IORD

V850E/MA1 pin 105: PCS2/_CS2/_IOWR

Emulator pin 102: PCS5/_CS5/_IOWR

Emulator pin 105: PCS2/_CS2/_IORD

2. IORD and IOWR inactive during normal access.

Ordinarily, IORD and IOWR signals become active during a read/write cycle and DMA fly-by transfer, but in this case they become active only during DMA fly-by transfer.

Workaround

1. Reverse IORD and IOWR in the target system.
2. None

No.4	SFR restriction

Details

1. Although bit 2 and 3 of the PMCT register are supposed to be fixed, they can be rewritten to 0.
2. Although bit 2 and 3 of the PMCCT register are supposed to be fixed, they can be rewritten to 0.
3. The initial value of the PMCCT register when started in ROM-less mode is 00h instead of F3h.
4. Port DL is always started in control mode immediately after starting the emulator.

Workaround

1. None. This restriction applies when using the IE-V850E-MC-A.
2. None. This restriction applies when using the IE-V850E-MC-A.
3. Write any bit to 1, if you want to use in control mode when starting in ROM-less mode. This restriction is not applicable to versions with control code D or later.
4. It is possible to change to port mode by writing 0 immediately after starting the ICE. This restriction is not applicable to versions with control code D or later

No.5	A/D converter operation enable bit

Details

A/D conversion may not start even if the A/D conversion operation enable bit (CE bit) of the A/D converter mode register 0 (ADM0) is set to 1.

Workaround

Set the ADM0 register two times consecutively.

No.6	Pin status restriction single chip mode 1 and ROM-less mode 0/1

Details

When Reset is performed in single chip mode 1, ROM-less mode 0 or 1, the prescribed pins will output a specific level without going into a high impedance state. (See Attachment 1.)

Workaround

None

No.7	DMA start by built-in peripheral I/O interrupt

Details

A DMA request is retained, while DMA transfer is prohibited (including abortion of NMI or forced termination by software), when DMA transfer is started by an interrupt from the integrated peripheral I/O. The retained request, however cannot be cleared. As a result, there is a possibility, that an interrupt set to trigger the start of DMA transfer will be generated, while DMA transfer is prohibited. If you do not want to start DMA transfer with this interrupt at a stage where DMA transfer is enabled, execute the instructions on the following workaround. In particular, please bear this in mind for cases, where one DMA channel is used with multiple applications (start factor is changed while in progress, etc.), DMA transfer is terminated in progress, or forcible termination.

Workaround

Take the following procedure:

1- Set DMA trigger factor register (DTFRn) to 00H to prohibit a DMA request from the integrated peripheral I/O.

2- To perform dummy DMA transfer, set the DMA source address register (DSAn) and the DMA destination address register (DDAn) to a region that does not influence the system.

3- Set the DMA transfer count register (DBCn) to 0000H.

4- Set the Enn bit and the STGn bit of the DMA channel control register (DCHCn) to 1, and perform dummy DMA transfer with the software trigger. When doing this, make sure that the MLEn bit of the same register is cleared to 0. This will ensure that dummy DMA transfer is generated along with a DMA transfer completion interrupt (INTDMAn), and the Enn bit will automatically clear to 0.

Note 1: If you do not want to generate a DMA transfer completion interrupt through dummy transfer, set the DMAMKn bit of interrupt control register (DMAICn) to 1 before generating dummy DMA transfer to mask the interrupt.

Note 2: If DMA transfer is reset by a DMA request from the integrated peripheral I/O after a DMA request is cleared, the first set the DSAn, DDAn, and DBCn registers, then set the DTFRn register and set the Enn bit of the DCHCn register.

Caution:

In response to the rstriction related to the DMA function, we have to added a bit (bit 7) to clear DMA requests by interrupts from the integrated peripheral I/O to the DMA trigger factor register 0-3 (DTFR0-3). NEC requests that your company consider implementing the appropriate changes to software. The specifications for the countermeasure are shown below. This information will be included in the next user's manual (2nd edition)

- DMA trigger factor register (DTFRn) n = 0 – 3

Reset value 00H

7	6	5	4	3	2	1	0
DFn	0	IFCn5	IFCn4	IFCn3	IFCn2	IFCn1	IFCn0

Newly added bit (Current specification: fixed at 0)
*bits 0 to 6 are the same as current specifications

DFn	DMA transfer request
0	No DMA transfer request
1	DMA transfer request

- The above register can be read or written in 8-bits units. Only bit 7 can be read or written in 1 or 8 bit units.
- access to bit 7 is only possible to write to 0

If a DMA transfer request has to be cleared, because an interrupt as a start condition for DMA transfer is generated and while DMA transfer is prohibited (abort by NMI or forced termination by software), clear the DFn bit after you have stopped the interrupt condition (example: disable receive line in the case of serial receiving).
It is unnecessary to stop an interrupt generation before the start of the next DMA transfer, if it is clear by the application that another interrupt will not occur.

No.8	DTOC read access

Details

Both read and write access should be possible on the DTOC register, however now only write access is possible.

Workaround

Treat the register as a read-only register.

No.9	SDRAM lead access

Details

A minimum data input setup time (tSDRMK) of 10ns is required for the rise of SDCLK when reading SDRAM. (The specification for this chip is 8ns.)

Workaround

Ensure a data input set up time (tSDRMK) of 10ns. Take particular care when using the emulator at 50 MHz. This will be corrected in IE-V850E-MC-A.

No.10	Restriction on external interrupt

Details

The INTPn0 pin cannot be used as an external interrupt pin.

Workaround

Set the CEn bit of timer control register Cn0 (TMCCn0) and start timer C.

This restriction has been removed in products with control code B or later.

No.11	Restriction on UART

Details

When the CAEn bit of asynchronous serial interface mode register n (ASIMn) is level is output from the TXDn pin. As a result, the transmission destination side will malfunction at UART activation.

Workaround

Set the port pin that has an alternate function with the TxDn pin to output port mode and output a high level from that pin. Then, set the CAEn bit to set 1 and set the port pin to the control mode (TxDn pin).

This restriction has been removed in products with control code B or later.

No.12	Illegal write access to interrupt control register

Details

When a write access is performed to an interrupt control register (FFFFF110H to FFFFF170H) or an interrupt mask register (FFFFF100H to FFFFF107H), the written value may be incorrect.
The occurrence of this restriction depends on the combination of the IE-V850E-MC-A and IE-703107-MC-EM1.

This effect does not occur in the combination of IE-V850E-MC-A with control code G or later and IE-703107-MC-EM1 with the control code D or later.

Workaround

Please contact the V850 product support group V850.support@ee.nec.de for further information.

No.13	A/D converter timer 1 trigger mode

Details

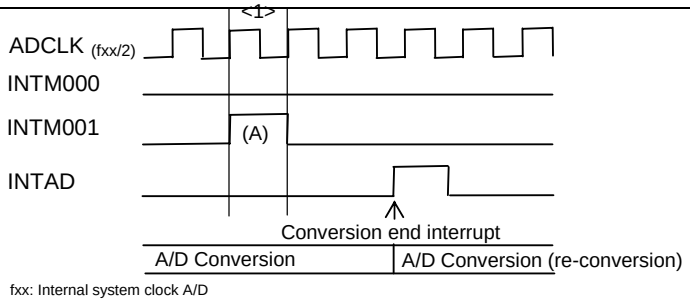
This restriction occurs, when in the timer 1 trigger mode or external trigger mode of the A/D converter is used (it does not occur when timer 4 trigger mode is used).
Originally, only INTM000 can be the trigger to start the A/D converter in the timer 1 trigger mode, and ADTRG pin input in the external trigger mode, therefor the interrupt sources listed below should be ignored. However, if one of the interrupt sources listed below occurs immediately before the end of A/D conversion (<1> in the figure below; 2 internal system clocks), it is mistakenly judged as the A/D conversion start trigger. As a result, A/D conversion is started again after the A/D conversion end interrupt (INTAD) is issued. The first A/D conversion ends correctly and the result is stored in the ADCRn register (this value can be read during the second conversion).
The restarted A/D converter performs the conversion operation correctly, issues the A/D conversion end interrupt (INTAD) and stops.

[Interrupt sources that can trigger A/D conversion]

Timer match interrupt	INTM001
	INTM010
	INTM011
External pin interrupt Note	INP001
	INTP010
	INTP011

Note
The external interrupt signal that functions alternately as the external capture trigger input of timer C (channel 0 and 1) can also be a trigger for re-conversion. In the case of an external interrupt input, the restriction occurs, when a valid edge is input before the timing of (A) in the figure below by the noise eliminator (analog delay (60 to 220 ns)).

[Example of timing at which this effect occurs]

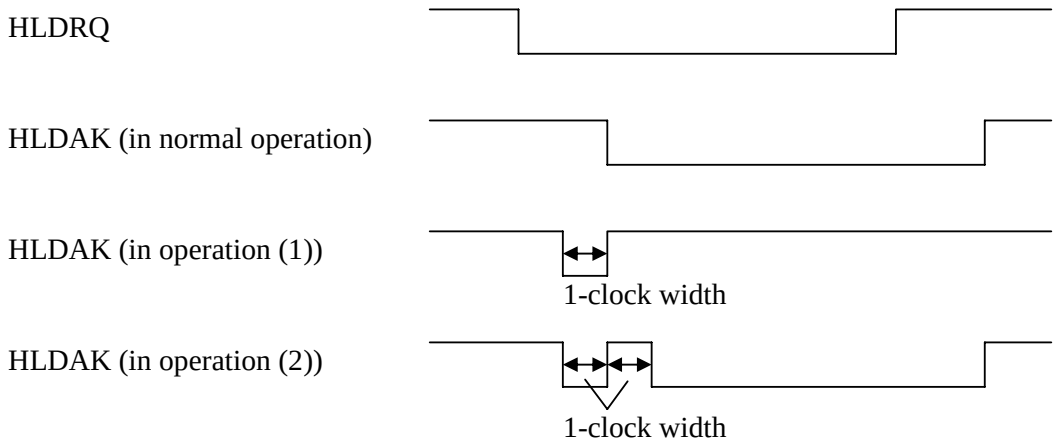


Condition:
The compare match interrupt (INTM001/010/011) of timer C (channel 0 and 1) does not occur during A/D conversion, and the external interrupt signal (INTP001010/011) is not input during A/D conversion.
This restriction does not occur when the A/D trigger mode or timer 4 trigger mode is used.

Workaround
Since the conversion result is correct even when this effect occurs, the affect of this restriction is small when obtaining the latest conversion value. If the re-conversion causes any problems, start A/D conversion in the A/D trigger mode by setting the ADCE bit of the ADM0 register to 1, in the interrupt service routine of the timer match interrupt.

No.14	HLDAK signal output

Details
The _HLDAK signal output from the emulator in response to the _HLDRQ signal from the target system may be illegal (there are two cases).
This restriction occurs only when output of the _HLDAK signal and refresh conflict.



Workaround
There is no workaround.
This restriction has been corrected in the IE-703107-MC-EM1 with control code E or later.

The function of JP4 that is provided in control code E (V1.33) is described below.

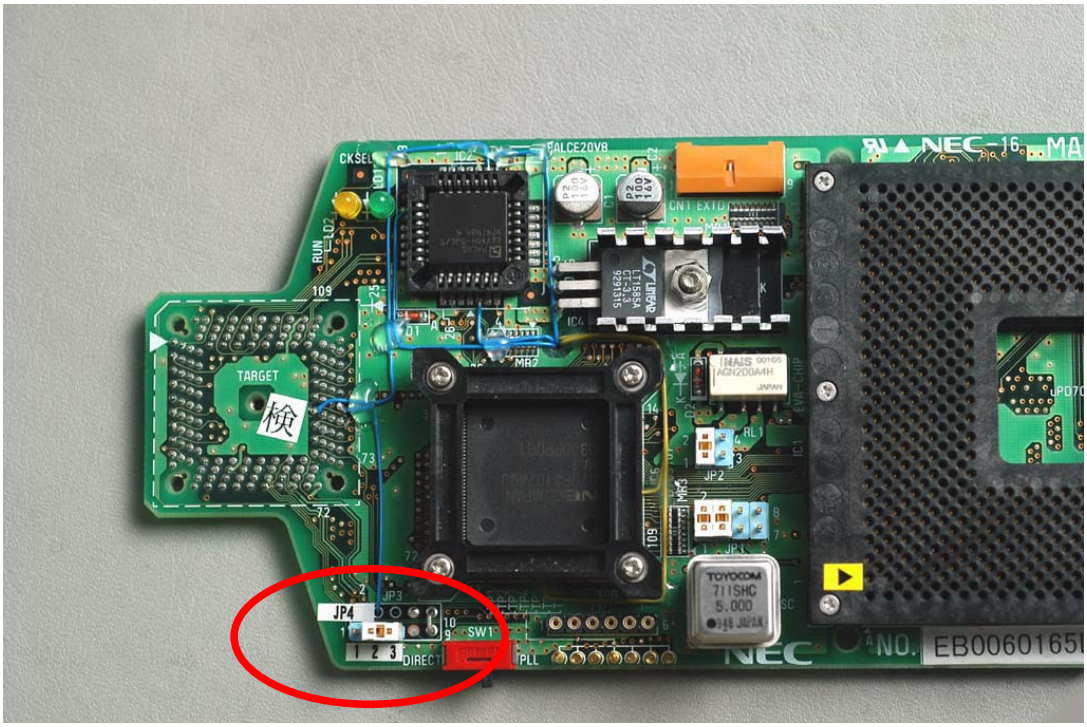
- Description of JP4 function

2-3 shorted: Setting to prevent _HLDAK illegal output
1-2 shorted: Setting functions other than above (factory setting)

(1) Set 2-3 shorted only for the following system.
- A system in which DRAM or SDRAM is connected to the external bus and the bus hold function is used.

(2) Set 1-2 shorted for systems other than above.
- A system in which DRAM or SDRAM is connected to the external bus and the bus hold function is not used.
- A system in which a device other than DRAM or SDRAM is connected to the external bus.
- A system which is used by the port function.

- JP4 position



(C)

Cautions

No.1	Continuous UART transfer

Details

The UART in this product has a two-stage buffer configuration consisting of a transmit buffer (TXBn) and a transmit shift register, each of it includes a status flag that indicates the status of the buffer (the TXBFn and TXSFn bits of the ASIFn register). If these two bits are read simultaneously, although ”10” changes to ”01”, depending on the timing, “11” or “00” may be inadvertently read out, because the timing at which “10” changes to “01” is in the period in which data is transferred from the transmit buffer to the transmit shift register. As a result, illegal operation may occur in a program that reads data from the TXBFn and TXSFn bits simultaneously.

Workaround

When performing continuous transmission, be sure to read only the ASIFn register’s TXBFn bit.

No.2	Refresh cycle SDRAM controller

Details

A refresh cycle may be executed for the SDRAM immediately after the RFNn bit of the SDRAM refresh control register (RFSn) is set (1: refresh operation enabled). However, operations during or immediately after the refresh cycle generated at that time, are not affected and that subsequent refresh cycle are executed normally at the set interval. (n = 1, 3, 4, 6)

Workaround

Operations during or immediately after the refresh cycle generated by the RFSn register’s setting are not affected, and subsequent refresh cycles are executed normally at the set interval. However, in applications in which this restriction occur, take workarounds by setting the RFSn register using the following procedure.

(1) Set the BTn1 and BTn0 bits of the BCTn register to01 (page ROM connected) while the Men bit is set (1). (n 0 0 to 7)
(2) Set the RENn bit of the RFSn register (1) to enable refresh. (n = 1, 3, 4, 6)
(3) Set the BTn1 bit of the BCTn register to 11 (SDRAM connected) while the Men bit is set (1). (n = 0 to 7)
(4) Set the SCRn register to initialize the SDRAM. (n = 1, 3, 4, 6)

(D) IE-V850E-MC-A Applicable Restrictions

The table below indicates whether or not the IE-V850E-MC-A restrictions are applicable during development.
As this table notes only if a restriction is applicable or not, please consult the to IE-V850E-MC-A limitation report TPS-HE-B-275x.

No.	Restrictions dependent on CPU functions	Applicable / not Applicable to V850E/MA1					
		Control Code					
		B	C	D	E	F	F
a-1	Interrupt aborts LD instruction immediately before JMP	✗	✗	✓	✓	✓	✓
a-2	Restriction on IRAM read access after start of interrupt servicing	✗	✗	✓	✓	✓	✓
a-3	Fetching is abnormal immediately after writing to SCRn register	✗	✗	✓	✓	✓	✓
a-4	Single, line, or single step transfer of 2-cycle DMA	✗	✗	✓	✓	✓	✓
a-5	Port C is not set in control mode immediately after starting in ROM-less mode	✗	✗	✓	✓	✓	✓
a-6	Restriction on port DH/DL	✗	✗	✓	✓	✓	✓
a-7	HLDAK output illegal due to conflict of self-refresh cycle and HOLDRQ in STOP mode	✗	✗	✓	✓	✓	✓
a-8	Fetch/data access fails if hardware STOP is executed after CBR refresh of DRAM/SDRAM	✗	✗	✓	✓	✓	✓
a-9	Restrictions on data cache	✓	✓	✓	✓	✓	✓
a-10	PFCCM register cannot be read	✗	✗	✓	✓	✓	✓
a-11	VSB bus and memory controller (NB85E500/501/502) cannot be used together	✓	✓	✓	✓	✓	✓
a-12	Restrictions on VSB bus signal	✓	✓	✓	✓	✓	✓
a-13	Restrictions on NPB bus signal	✓	✓	✓	✓	✓	✓
a-14	Restrictions on memory controller (NB85E500) signal	✗	✗	✓	✓	✓	✓
a-15	Restrictions on instruction cache	✓	✓	✓	✓	✓	✓
a-16	Restrictions related to SDRAM access during bus hold	✗	✗	✓	✓	✓	✓
a-17	Restrictions on self-refresh cycle by SELFREF pin	✗	✗	✓	✓	✓	✓
a-18	Restrictions related to flyby DMA transfer to EDO DRAM	✗	✗	✓	✓	✓	✓
a-19	Restrictions on EDO DRAM with idle state inserted	✗	✗	✓	✓	✓	✓
a-20	Restrictions related to flyby DMA transfer	✗	✗	✓	✓	✓	✓
a-21	Restrictions of pin status in single-step mode 1 and ROMless mode 0 and 1	✗	✗	✓	✓	✓	✓

a-22	Incorrect write-back with LD/SLD instructions when executing CALLT/SWITCH instruction	✗	✗	✗	✓	✓	✓
a-23	Restriction on use of external bus when the product is employed as an emulator for the V850E/IA1	✓	✓	✓	✓	✓	✓
a-24	Restriction related to the output of the _DMAAK signal	✗	✗	✗	✓	✓	✓
a-25	Restriction related to starting DMA by built in-in peripheral I/O interrupt	✗	✗	✗	✓	✓	✓
a-26	Restriction related to EDO DRAM bus collision	✗	✗	✗	✓	✓	✓
a-27	Restriction on the 2-way associative function of the instruction cache	✓	✓	✓	✓	✓	✓
a-28	Forced stop of external DMA transfer in DMA line transfer mode	✓	✓	✓	✓	✓	✓
a-29	Restriction on reading the DCHC register when DMA 2-cycle transfer is completed	✗	✗	✗	✓	✓	✓
a-30	Restriction related to conflict between SDRAM initialization and SELFREF input	✗	✗	✗	✓	✓	✓
a-31	Restriction on half word writing to BSC, BCC, DWC0 and DWC1 registers	✗	✗	✗	✓	✓	✓
a-32	Restriction related to SDRAM write operation	✗	✗	✗	✓	✓	✓
a-33	Restrictions on DRAM fetch immediately after block DMA transfer from DRAM to internal RAM	✗	✗	✓	✓	✓	✓
a-34	Restrictions on instruction cache 2	✓	✓	✓	✓	✓	✓
a-35	Restriction on SLD instruction	✗	✗	✗	✗	✓	✓
a-36	I/O cannot be used when using VSB bus	✓	✓	✓	✓	✓	✓
a-37	Restriction on instruction cache 3	✓	✓	✓	✓	✓	✓
a-38	Restriction on DMAAK signal during DMA line transfer.	✓	✓	✓	✓	✓	✓
a-39	Restriction caused by interrupt input during execution of bit manipulation instruction.	✗	✗	✗	✗	✓	✓
a-40	Restriction on hardware stop during bit manipulation instruction execution.	✓	✓	✓	✓	✓	✓
a-41	Restriction related to interrupt od DMA transfer by external cause.	✗	✗	✗	✗	✓	✓
a-42	Restriction on SDCKE signal during bus hold.	✗	✗	✗	✗	✗	✓
a-43	Caution regarding SDRAM controller	✗	✗	✗	✗	✗	✗
a-44	Restriction on mul/mulu instruction	✗	✗	✗	✗	✗	✗
a-45	Restriction on Page ROM access	✗	✗	✗	✗	✗	✗
a-46	DMA transfer forcible termination	✗	✗	✗	✗	✗	✗
a-47	DMA is forcible suspended by NMI	✗	✗	✗	✗	✗	✗
a-48	Program execution and DMA transfer in internal RAM	✗	✗	✗	✗	✗	✗
a-49	DAM transfer whose transfer count is set to two (part1)	✗	✗	✗	✗	✗	✗

a-50	DAM transfer whose transfer count is set to two (part2)	✗	✗	✗	✗	✗	✗
a-51	TCn bit of DMA is not cleared automatically	✗	✗	✗	✗	✗	✗

✓: Not applicable
✗: applicable

No.	Restrictions dependent on debug functions	Applicable / not Applicable to V850E/MA1					
		Control Code					
		B	C	D	E	F	G
b-1	Restriction on operating frequency	✗	✗	✗	✓	✓	✓
b-2	Restriction on break timing when guard area is fetched	✗	✗	✓	✓	✓	✓
b-3	Restriction on trace in case of miss-alignment (during read access only)	✗	✗	✓	✓	✓	✓
b-4	Restrictions on trace data on execution of HALT or STOP instruction	✗	✗	✓	✓	✓	✓
b-5	Bit manipulation instruction (set1, clr1, not1, tst1) access data is illegally traced by tracer.	✗	✗	✓	✓	✓	✓
b-6	Events including data conditions by access of bit manipulation instruction cannot be detected	✗	✗	✓	✓	✓	✓
b-7	Restriction on HOLD status	✗	✗	✓	✓	✓	✓
b-8	ROM contents are rewritten if emulation ROM area is accessed for write	✗	✗	✗	✗	✗	✗
b-9	Restriction on SFR illegal break	✓	✓	✓	✓	✓	✓
b-10	Restriction on programmable I/O space	✗	✗	✗	✗	✗	✗
b-11	Break does not occur even if breakpoint is set	Supported by debugger					
b-12	Restriction related to access address during DMA trace	✗	✗	✗	✗	✗	✗
b-13	Restriction on DBPC and DBPSW access during a break	✗	✗	✗	✗	✗	✗
b-14	Restriction on DBTRAP instructions	✗	✗	✗	✗	✗	✗
b-15	Restriction on illegal guard break when IRAM size is 28kB	✗	✗	✗	✗	✓	✓
b-16	Restriction on illegal trace when big endian is used	✗	✗	✗	✗	✓	✓
b-17	Restriction on access data traced by DMA	✗	✗	✗	✗	✗	✗
b-18	Restriction on SFR read access during break	✗	✗	✗	✗	✗	✗

✓ : Not applicable
✗ : applicable

Attachment 1

Operating Status / Pin	Current Status	After Change
	Reset (Single-chip mode 1, ROMless mode 0,1)	Reset (Single-chip mode 1, ROMless mode 0,1)
A0-A15（PAL0-PAL15）	L	Hi-Z
A16-A25（PAH0-PAH9）	L	Hi-Z
D0-D15（PDL0-PDL15）	L	Hi-Z
$\overline{CS0}$-$\overline{CS7}$（PCS0-PCS7）	H	Hi-Z
$\overline{RAS1}$, $\overline{RAS3}$, $\overline{RAS4}$, $\overline{RAS6}$ （PCS1, PCS3, PCS4, PCS6）	–	–
$\overline{IOWR}$（PCS2）	–	–
$\overline{IORD}$（PCS5）	–	–
$\overline{LWR}$, $\overline{UWR}$（PCT0, PCT1）	H	Hi-Z
$\overline{LCAS}$, $\overline{UCAS}$（PCT0, PCT1）	–	–
LDQM, UDQM（PCT0, PCT1）	–	–
$\overline{RD}$（PCT4）	H	Hi-Z
$\overline{WE}$（PCT5）	H	Hi-Z
$\overline{OE}$（PCT6）	H	Hi-Z
$\overline{BCYST}$（PCT7）	H	Hi-Z
$\overline{WAIT}$（PCM0）	H	Hi-Z
CLKOUT（PCM1）	Operates	Operates
BUSCLK（PCM1）	–	–
$\overline{HLDAK}$（PCM2）	H	Hi-Z
$\overline{HLDRQ}$（PCM3）	–	Hi-Z
$\overline{REFRQ}$（PCM4）	H	Hi-Z
SELFREF（PCM5）	–	Hi-Z
SDCKE（PCD0）	L	Hi-Z
SDCLK（PCD1）	Operates	Hi-Z
$\overline{SDCAS}$（PCD2）	–	–
$\overline{LBE}$（PCD2）	H	Hi-Z
$\overline{SDRAS}$（PCD3）	–	–
$\overline{UBE}$（PCD3）	H	Hi-Z
$\overline{DMAAK0}$-$\overline{DMAAK3}$(PBD0-PBD3)	H	Hi-Z

Remark Hi-z : High impedance
H : High-level output
L : Low-level output
- : Input non-sampling

(E) Valid Specification

Item	Date published	Document No.	Document Title
1	September 2003	U14481EJ2V0UM00.pdf	IE-703107-MC-EM1 User's Manual

(F) Revision History

Item	Date published	Document No.	Comment
1	Oct. 2000	IE-703107-HE-B-2760	Initial issue
2	Jan. 2001	IE-703107-HE-B-2761	- Added control code B to table of precautions. - Update restriction 1, 3, 4, 5, 6, 7, 8. - - Added chapter IE-V850E-MC-A Applicable Restrictions
3	Jan. 2002	IE-703107-HE-B-2762	- Added control code C to table of precautions - Added restrictions 10, 11 - Update Chapter IE-V850E-MC-A Applicable Restrictions
4	Sep 2003	IE-703107-HE-B-2763	- Added control code C to table of precautions - Added restrictions 10, 11 - Update Chapter IE-V850E-MC-A Applicable Restrictions - Added chapter Cautions
5	Jun 2004	IE-703107-HE-B-2774	- New doc. number, due to double numbering - Added control code E to table of precautions - Added restrictions 14