

**Customer Notification**

**μPD78F9222 Subseries**

**8-Bit Single-Chip Microcontrollers**

**Operating Precautions**

---

**μPD78F9221**

**μPD78F9222**

## **DISCLAIMER**

The related documents in this customer notification may include preliminary versions. However, preliminary versions may not have been marked as such.

The information in this customer notification is current as of its date of publication. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC PRODUCT(S). Not all PRODUCT(S) and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.

No part of this customer notification may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this customer notification. NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC PRODUCT(S) listed in this customer notification or any other liability arising from the use of such PRODUCT(S).

No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others. Descriptions of circuits, software and other related information in this customer notification are provided for illustrative purposes of PRODUCT(S) operation and/or application examples only. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.

While wherever feasible, NEC endeavors to enhance the quality, reliability and safe operation of PRODUCT(S) the customer agree and acknowledge that the possibility of defects and/or erroneous thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects and/or errors in PRODUCT(S) the customer must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.

The customer agrees to indemnify NEC against and hold NEC harmless from any and all consequences of any and all claims, suits, actions or demands asserted against NEC made by a third party for damages caused by one or more of the items listed in the enclosed table of content of this customer notification for PRODUCT(S) supplied after the date of publication.

### **Applicable Law:**

The law of the Federal Republic of Germany applies to all information provided by NEC to the Customer under this Operating Precaution document without the possibility of recourse to the Conflicts Law or the law of 5th July 1989 relating to the UN Convention on Contracts for the International Sale of Goods (the Vienna CISG agreement).

Düsseldorf is the court of jurisdiction for all legal disputes arising directly or indirectly from this information. NEC is also entitled to make a claim against the Customer at his general court of jurisdiction.

If the supplied goods/information are subject to German, European and/or North American export controls, the Customer shall comply with the relevant export control regulations in the event that the goods are exported and/or re-exported. If deliveries are exported without payment of duty at the request of the Customer, the Customer accepts liability for any subsequent customs administration claims with respect to NEC.

**Notes:** (1) "**NEC**" as used in this statement means NEC Corporation and also includes its direct or indirect owned or controlled subsidiaries.

(2) "**PRODUCT(S)**" means 'NEC semiconductor products' (*NEC semiconductor products* means any semiconductor product developed or manufactured by or for NEC) and/or 'TOOLS' (*TOOLS* means 'hardware and/or software development tools' for NEC semiconductor products' developed, manufactured and supplied by 'NEC' and/or 'hardware and/or software development tools' supplied by NEC but developed and/or manufactured by independent 3<sup>rd</sup> Party vendors worldwide as their own product or on contract from NEC)

## Table of Contents

(A)	Table of Operating Precautions .....	4
(B)	Description of Operating Precautions.....	5
(C)	Valid Specification.....	7
(D)	Revision History .....	8

μPD78F9222 Subseries

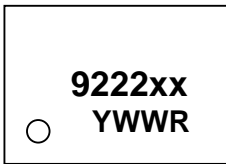
**(A) Table of Operating Precautions**

No.	Outline	μPD78F922x			
		Rev. <sup>Note</sup>	2.2	2.3	
		Rank <sup>Note</sup>	K	E	P
1	Restriction for STOP mode (Technical Limitation)	X	X	✓	
2	Restriction on using flash self-programming (Direction of use)	X	X	X	

✓ : Not applicable  
 X : applicable

**Note:** -The version is indicated by the in the lot number, marked on each product.  
 Pls. refer to the below marking on each package.  
 - Older device versions are not part of this customer notification, because it is expected that they are not used anymore.

Marking for versions below V2.3

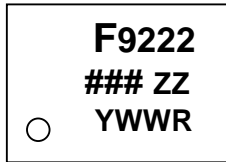


xx: DS or ES  
 Y: Year Code  
 WW: Week Code  
 R: Rank

**μPD78F9221/2**

Revision	Marking
V 2.2 (ES)	F9222 V22ES 448K
V 2.3	F9221 xxxE F9222 xxxE

Marking for versions V2.3 or later



###: Code Number (only preprogrammed flash)  
 ZZ: Flash Grade  
 Y: Year Code  
 WW: Week Code  
 R: Rank

**(B) Description of Operating Precautions**

No. 1	Restriction for STOP mode (Technical Limitation)
	<p><u>Details</u></p> <p>When CPU execute STOP instruction with IE flag = 0(DI instruction executed) and IF flag = 1 that is not masked, STOP mode will not be released. Then any other interrupts are occurred, STOP mode is not released, either.</p> <p>Case 1 : When CPU execute STOP instruction with IE flag = 0 and IF flag = 1, MK flag = 0. DI ; Interrupt is disabled SET1 PIF0 ; Set interrupt request flag(INTP0) CLR1 PMK0 ; Clear interrupt mask flag(INTP0) SET1 P2.0 ; Set Port20 to "1" STOP ; Changing STOP mode CLR1 P2.0 ; Clear Port20(Will not be executed)</p> <p>When interrupt enabled and standby release signal is occurred, and CPU execute interrupt request pending instruction right before STOP instruction executing, then STOP mode will not be released.</p> <p>Case2 : When CPU execute STOP instruction with IE flag = 1 and IF flag = 1, MK flag = 0. EI ; Interrupt is enabled SET1 P2.0 ; Set Port20 to "1" SET1 PIF0 ; Set interrupt request flag(INTP0) CLR1 PMK0 ; Executing interrupt request pending instruction STOP ; Changing STOP mode CLR1 P2.0 ; Clear Port20(Never executed)</p> <p>Note : interrupt request pending instruction Write access instruction for interrupt request flag register 0 (IF0) Write access instruction for interrupt mask flag register 0 (MK0)</p> <p><u>Workaround</u></p> <p>Execute EI instruction before STOP instruction execution. Then do not execute Interrupt request pending instruction right before STOP execution.</p> <p>Case3 : Executing EI instruction right before STOP instruction. DI ; Interrupt disabled SET1 PIF0 ; Set interrupt request flag(INTP0) CLR1 PMK0 ; Clear interrupt mask flag(INTP0) SET1 P2.0 ; Set Port20 to "1". EI ; Interrupt enabled STOP ; Changing STOP mode CLR1 P2.0 ; Clear Port20(will execute)</p> <p>Note: If interrupt is occurred before executing STOP instruction, it's necessary to generate interrupt for releasing from STOP mode because interrupt request flag is cleared before executing STOP instruction.</p>

No. 2	Restriction on using flash self-programming (Direction of use)
<p><u>Details</u> If the standby function performed by the HALT instruction and flash self-programming are used together using the procedure shown below, the subsequent operation becomes unexpected.</p> <p><u>Workaround</u> When using flash self-programming, clear the FLCMD register to 0 immediately before shifting to normal mode or self-programming mode. In addition, execute NOP and HALT instructions after specific sequence processing to shift to self-programming mode.</p> <p><u>Detailed explanation</u> The following two modes are available in these products.</p> <ul style="list-style-type: none"> <li>- Normal mode: The state in which normal operation is executed. Operation enters into a standby state after execution of the HALT instruction.</li> <li>- Self-programming mode: The state in which self-programming commands are executable. After setting commands, addresses and write data and executing the HALT instruction, self-programming is executed. The specific sequence described in this document is referring to the register manipulation to switch these two modes.</li> </ul> <p style="text-align: center;"><b>Process Leading up to Unexpected Operation</b></p> <p>The diagram illustrates the timing of various signals during a transition between modes. The top horizontal axis is divided into eight stages by vertical dashed lines. The signals are as follows:</p> <ul style="list-style-type: none"> <li><b>HALT instruction:</b> High during 'Normal HALT execution' and 'Normal HALT execution' stages.</li> <li><b>HALT execution flag:</b> High during 'Normal HALT execution' and 'Normal HALT execution' stages. Annotations &lt;1&gt; and &lt;5&gt; are placed at the start and end of these pulses.</li> <li><b>FLSPM:</b> High during 'Shift to SELF' and 'Command setting' stages. Annotation &lt;2&gt; is at the start, and &lt;4&gt; is at the end.</li> <li><b>SELF execution status:</b> High during 'SELF execution' and 'End of SELF' stages. Annotation &lt;3&gt; is at the start, and &lt;6&gt; is at the end.</li> <li><b>FLCMD register value:</b> 00H during 'Normal HALT execution' and 'Shift to SELF' stages. 'Any command value' during 'Command setting', 'SELF execution', and 'End of SELF' stages.</li> </ul>	

- <1>An ordinary HALT instruction is executed and the internal HALT execution flag is set. Self-programming is executed by setting the FLSPM bit while the HALT execution flag is set.
- <2>The specific sequence is executed and the operation then enters into self-programming mode. At this time, the FLSPM bit changes to indicate that self-programming is now executable. However, self-programming commands are not executed at this time, because the FLCMD register has been initialized to 00H.
- <3>Once a command value is set to the FLCMD register and the HALT instruction is executed, the self-programming command is executed. The HALT execution flag is cleared just as the self-programming command is executed.
- <4>Execution of the self-programming command is completed, the specific sequence is executed again, and operation enters into normal mode.
- <5>The HALT instruction is executed again, operation enters into standby, and the HALT execution flag is set.
- <6>After the standby state is released, the specific sequence is executed to shift to self-programming mode. If the command value set to the FLCMD register has not been initialized at this time, the command still set to the FLCMD register is reexecuted when the FLSPM bit is set. Self-programming is subsequently executed during CPU operation and the CPU fetches an incorrect instruction from the flash memory, resulting in an unexpected operation.

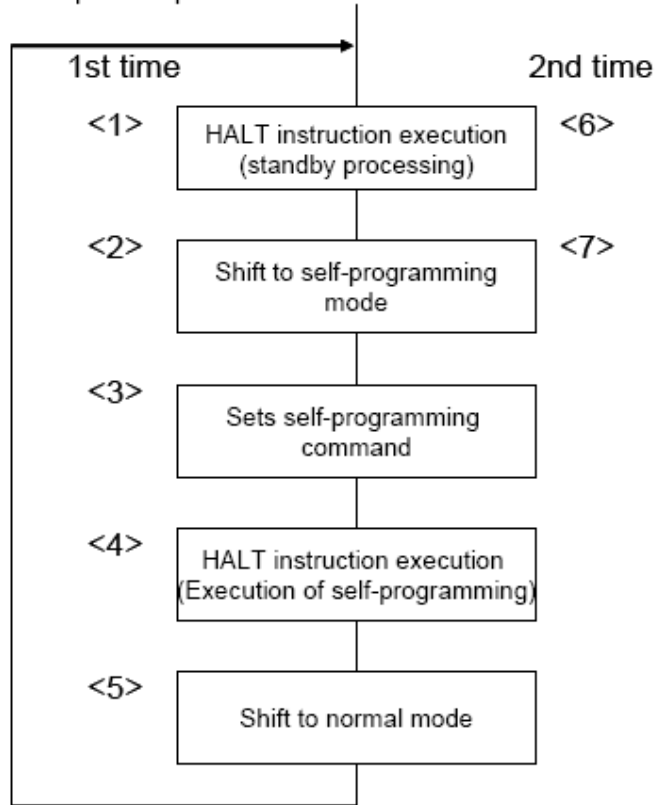
**Remark** The same situation occurs when flash self-programming is executed before <1>.

Workaround:

When using flash self-programming, clear the FLCMD register to 0 immediately before shifting to normal mode or self-programming mode; this prevents execution of illegal commands immediately after the mode is shifted. In addition, execute NOP and HALT instructions after specific sequence processing to shift to self-programming mode; this controls the execution timing between the CPU and the flash memory control block.

The flowcharts and source code examples for the operation restriction and its workaround implementation are described on the following pages.

Flowchart leading up to unexpected operation:



- <1>An ordinary HALT instruction is executed to shift to standby. After that, the standby state is released by a standby release signal, such as an interrupt.
- <2>The specific sequence is executed to shift to self-programming mode.
- <3>A self-programming command (block erase in the source code example) is set to the FLCMD register.
- <4>The self-programming command is executed by executing the HALT instruction.
- <5>After self-programming processing specified in <3> is completed, the specific sequence is executed to shift to normal mode. This example presumes that processes from <1> to <5> are performed repeatedly.
- <6>An ordinary HALT instruction is executed to generate a standby release signal, and the standby state is released.
- <7>A self-programming command (block erase in the source code example) is executed immediately after the specific sequence is executed to shift to self-programming mode for the second time. Consequently, microcontroller operation becomes unexpected.



Example source code causing unexpected operation (assembly language):

```

MAINLOOP:
    ; Executes HALT to shift to standby state - <1> and <6> in flowchart
    HALT

    ; Saves the interrupt mask setting before executing self-programming.
    DI                ; Disables interrupts
    MOV    A,MK0      ; Saves interrupt mask setting
    XCH   A,X
    MOV    A,MK1      ; Saves only MK0 in KU1+ and KY1+
    PUSH  AX
    MOV    MK0,#0FFH
    MOV    MK1,#0FFH

    ; Executes the specific sequence to shift to self-programming mode - <2> and <7> in flowchart
ModeOnLoop:
    MOV    PFCMD,#0A5H ; Controls PFCMD register
    MOV    FLPMC,#01H  ; Controls FLPMC register (set value)
    MOV    FLPMC,#0FEH ; Controls FLPMC register (inverted set value)
    MOV    FLPMC,#01H  ; Sets self-programming mode
    ;When using a clock generated by an external resonator or external input clock,insert a 16  $\mu$ s wait.
    ; Operation becomes unexpected when entered into self-programming mode for the second time.
    BT     PFS.0,$ModeOnLoop ; Confirms completion of mode shift

    ; Performs command settings - <3> in flowchart
    MOV    A, #0FH
    MOV    FLAPH,A      ; Sets number of block to be erased
    MOV    FLAPHC,A    ; Sets compare number for block to be erased (value set to FLAPH)
    MOV    FLCMD,#03H  ; Sets flash control command (block erase)
    MOV    PFS,#00H   ; Clears flash status register
    MOV    WDTE,#0ACH ; Clears and starts WDT

    ; Executes erase command - <4> in flowchart
    HALT ; Executes self-programming

    ; Executes the specific sequence to shift to normal mode - <5> in flowchart
ModeOffLoop:
    MOV    PFS,#00H
    MOV    PFCMD,#0A5H ; Controls PFCMD register
    MOV    FLPMC,#00H  ; Controls FLPMC register (set value)
    MOV    FLPMC,#0FFH ; Controls FLPMC register (inverted set value)
    MOV    FLPMC,#00H  ; Sets normal mode
    BT     PFS.0,$ModeOffLoop ; Confirms completion of mode shift
    POP   AX           ; Restores interrupt mask setting
    MOV   MK1,X
    XCH  A,X
    MOV  MK0,A
    BR   MAINLOOP
    
```

Example source code causing unexpected operation (C language):

```

while(1){
  /* Executes HALT to shift to standby state - <1> and <6> in flowchart */
  HALT();

  /* Saves interrupt mask settings */
  DI(); // Disables interrupts
  ch_mask_bak0 = MK0; // Saves only MK0 in KU1+ and KY1+
  ch_mask_bak1 = MK1; // ch_mask_bak0/1 are variables for saving

  /* Shifts to self-programming mode - <2> and <7> in flowchart */
  do{
    PFS = 0; // Clears flash status register
    PFCMD = 0xA5; // Controls PFCMD register
    FLPNC = 0x01; // Controls FLPNC register (set value)
    FLPNC = 0xFE; // Controls FLPNC register (inverted set value)
    FLPNC = 0x01; // Sets self-programming mode

    /* When using a clock generated by an external resonator or external input clock,
    insert a 16  $\mu$ s wait.*/

    /* Operation becomes unexpected when entered into self-programming mode
    for the second time. */

  }while(PFS.0 == 1); // Confirms completion of mode shift

  /* Performs command settings - <3> in flowchart */
  FLAPH = FLAPHC = 0x0F; // Specifies block to be erased
  FLCMD = 0x03; // Specifies erase command
  PFS = 0x00; // Clears flash status register
  WDTE = 0xAC; // Clears WDT counter

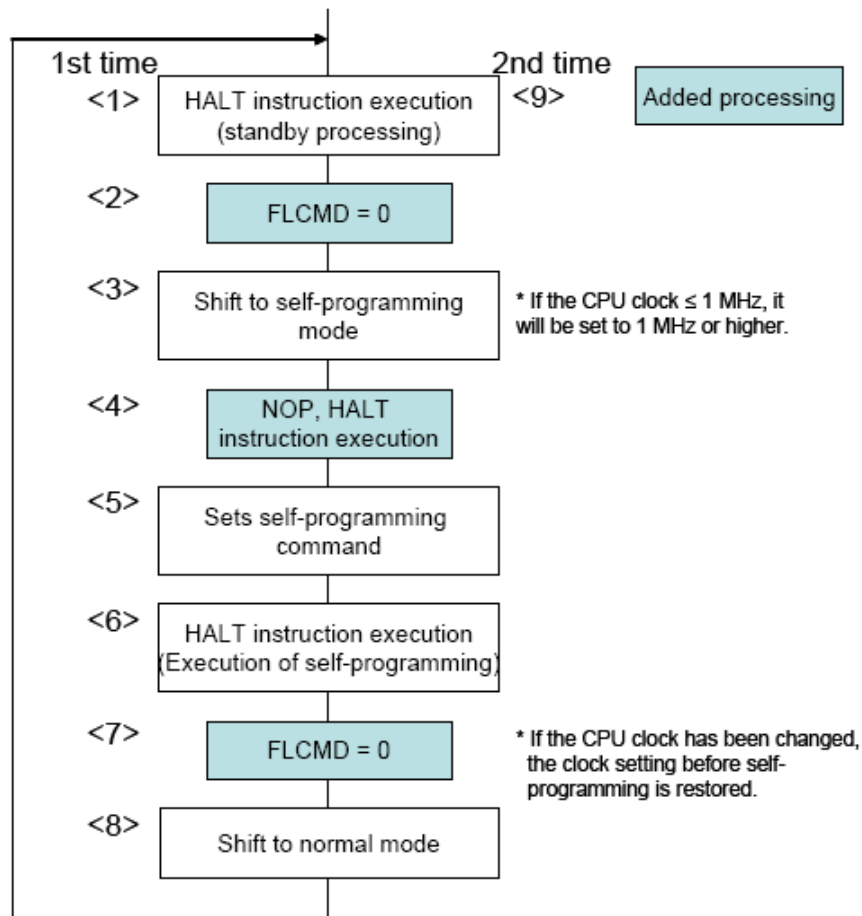
  /* Executes erase command - <4> in flowchart */
  HALT(); // Executes erase command

  /* Shifts to normal mode - <5> in flowchart */
  do{
    PFS = 0; // Clears flash status register
    PFCMD = 0xA5; // Controls PFCMD register
    FLPNC = 0x00; // Controls FLPNC register (set value)
    FLPNC = 0xFF; // Controls FLPNC register (inverted set value)
    FLPNC = 0x00; // Sets normal mode
  }while(PFS.0 == 1); // Confirms completion of mode shift

  /* Restores interrupt mask settings */
  MK0 = ch_mask_bak0;
  MK1 = ch_mask_bak1;
}

```

Flowchart of workaround implementation:



- <1>An ordinary HALT instruction is executed to shift to standby. After that, the standby state is released by a standby release signal, such as an interrupt.
- <2>The FLCMD register is cleared to 0 before executing the specific sequence to shift to self-programming mode. The CPU clock is set to 1 MHz or higher.
- <3>The specific sequence is executed to shift to self-programming mode.
- <4>After the specific sequence (1 assigned to FLPMC for the second time), NOP and HALT instructions are executed. It takes at most 10  $\mu$ s until the HALT instruction is released.
- <5>A self-programming command (such as write or erase) is set to the FLCMD register.
- <6>The self-programming command is executed by executing the HALT instruction.
- <7>The FLCMD register is cleared to 0 before the specific sequence is executed to shift to normal mode.
- <8>Execute the specific sequence to shift to normal mode. If the CPU clock has been changed, the clock setting before self-programming is restored at this time.
- <9>This restriction is avoided by adding the above processes <2>, <4>, <7> and <8>.

Example of source code to which workaround is implemented (assembly language):

```

MAINLOOP:
    ; Executes HALT to shift to standby state - <1> and <9> in flowchart
    HALT

    ; Saves the interrupt mask setting before executing self-programming.
    DI                ; Disables interrupts
    MOV A,MK0         ; Saves interrupt mask setting
    XCH A,X
    MOV A,MK1         ; Saves only MK0 in KU1+ and KY1+
    PUSH AX
    MOV MK0, #0FFH
    MOV MK1, #0FFH

    ; Initializes FLCMD register - <2> in flowchart
    MOV FLCMD, #00H
    ; If CPU clock is 1 MHz, sets CPU clock to 1 MHz or higher.

    ; Executes the specific sequence to shift to self-programming mode - <3> in flowchart
ModeOnLoop:
    MOV PFCMD,#0A5H   ; Controls PFCMD register
    MOV FLPMC,#01H   ; Controls FLPMC register (set value)
    MOV FLPMC,#0FEH  ; Controls FLPMC register (inverted set value)
    MOV FLPMC,#01H   ; Sets self-programming mode
    BT PFS.0,$ModeOnLoop ; Confirms completion of mode shift

    ; Executes NOP and HALT instructions - <4> in flowchart
    NOP
    HALT
    ;When using a clock generated by an external resonator or external input clock, insert an 8us wait

    ; Performs command settings - <5> in flowchart
    MOV A, #0FH
    MOV FLAPH,A      ; Sets number of block to be erased
    MOV FLAPHC,A     ; Sets compare number for block to be erased (value set to FLAPH)
    MOV FLCMD,#03H  ; Sets flash control command (block erase)
    MOV PFS,#00H    ; Clears flash status register
    MOV WDTE,#0ACH  ; Clears and starts WDT
    ; Executes erase command - <6> in flowchart
    HALT            ; Executes self-programming

    ; Initializes FLCMD register - <7> in flowchart
    MOV FLCMD, #00H
    ; If the CPU clock has been changed, the setting before self-programming is restored.

    ; Executes the specific sequence to shift to normal mode - <8> in flowchart
ModeOffLoop:
    MOV PFS,#00H
    MOV PFCMD,#0A5H ; Controls PFCMD register
    MOV FLPMC,#00H ; Controls FLPMC register (set value)
    MOV FLPMC,#0FFH ; Controls FLPMC register (inverted set value)
    MOV FLPMC,#00H ; Sets normal mode
    BT PFS.0,$ModeOffLoop ; Confirms completion of mode shift
    POP AX          ; Restores interrupt mask setting
    MOV MK1,X
    XCH A,X
    MOV MK0,A
    BR MAINLOOP
    
```

Example of source code to which workaround is implemented (C language):

```

while(1){
    /* Executes HALT to shift to standby state - <1> and <9> in flowchart */
    HALT();

    /* Saves interrupt mask settings */
    DI();          // Disables interrupts
    ch_mask_bak0 = MK0; // Saves only MK0 in KU1+ and KY1+
    ch_mask_bak1 = MK1; // ch_mask_bak0/1 are variables for saving

    /* Initializes FLCMD register - <2> in flowchart */
    FLCMD = 0;
    /* If CPU clock  $\delta$  1 MHz, sets CPU clock to 1 MHz or higher */

    /* Enters into self-programming mode - <3> in flowchart */
    do{
        PFS = 0; // Clears flash status register
        PFCMD = 0xA5; // Controls PFCMD register
        FLPMC = 0x01; // Controls FLPMC register (set value)
        FLPMC = 0xFE; // Controls FLPMC register (inverted set value)
        FLPMC = 0x01; // Sets self-programming mode
    }while(PFS.0 == 1); // Confirms completion of mode shift

    /* Executes NOP and HALT instructions - <4> in flowchart */
    NOP();
    HALT();
    /* When using a clock generated by an ext. resonator or external input clock, insert an 8 $\mu$ s wait. */

    /* Performs command settings - <5> in flowchart */
    FLAPH = FLAPHC = 0x0F; // Specifies block to be erased
    FLCMD = 0x03; // Specifies erase command
    PFS = 0x00; // Clears flash status register
    WDTE = 0xAC; // Clears WDT counter

    /* Executes erase command - <6> in flowchart */
    HALT(); // Executes erase command

    /* Initializes FLCMD register - <7> in flowchart */
    FLCMD = 0;
    /* If the CPU clock has been changed, the setting before self-programming is restored. */

    /* Shifts to normal mode - <8> in flowchart */
    do{
        PFS = 0; // Clears flash status register
        PFCMD = 0xA5; // Controls PFCMD register
        FLPMC = 0x00; // Controls FLPMC register (set value)
        FLPMC = 0xFF; // Controls FLPMC register (inverted set value)
        FLPMC = 0x00; // Sets normal mode
    }while(PFS.0 == 1); // Confirms completion of mode shift

    /* Restores interrupt mask settings */
    MK0 = ch_mask_bak0;
    MK1 = ch_mask_bak1;
}

```

**(C) Valid Specification**

<b>Item</b>	<b>Date published</b>	<b>Document No.</b>	<b>Document Title</b>
1	July 2005 or later	U16898EJ...	User's Manual

**(D) Revision History**

<b>Item</b>	<b>Date published</b>	<b>Document No.</b>	<b>Comment</b>
1	January 21, 2005	TPS-LE-OP-F9222-1	1 <sup>st</sup> Release
2	March 07, 2005	TPS-LE-OP-F9222-2	2 <sup>nd</sup> Release addition of version V 2.1 and later
3	March 22, 2006	TPS-LE-OP-F9222-3	3 <sup>rd</sup> Release addition of Rank "P"
4	May 2007	U18766EE1V0IF00	4 <sup>th</sup> Release, addition of restriction 2, removal of old versions, new doc no