NEC

Customer Notification

μPD780948 Subseries
μPD780948A Subseries™

8-bit Single-Chip Microcontrollers

Operating Precautions

μPD780948
μPD78F0948
μPD780948A
μPD78F0948A

Document No. TPS-LE-OP-F0948A-2 (3rd edition)
Date Published March 2005

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µPD780948 and µPD780948A Subseries

(A) Table of Operating Precautions

No.	Outline		µPD78F0948			µPD780948
		Rev.	V4.0	V5.1	V6.0	V3.0
		Rank Note	E	X, M	H, W	E
1	DCAN The compare state machine for frame reception (Technical Limitation)		✗	✓	✓	✓
2	DCAN Change from Error Active State to Error Passive State during error frames (Technical Limitation)		✗	✓	✓	✓
3	DCAN Hard synchronization during all required situations (Technical Limitation)		✗	✓	✓	✓
4	DCAN Hard synchronization instead of soft synchronization (Technical Limitation)		✗	✓	✓	✓
5	DCAN Suspend transmission operation (Technical Limitation)		✗	✓	✓	✓
6	DCAN REDEF Limitation (Technical Limitation)		✗	✗	✗	✗
7	DCAN SLEEP request (Technical Limitation)		✗	✗	✗	✗
8	DCAN Initialization of TXA bits (Technical Limitation)		✗	✗	✗	✗
9	DCAN Sample point Timing, Glitch Detection and Resynchronization (Technical Limitation)		✗	✗	✗	✗
10	DCAN Resynchronization (Technical Limitation)		✗	✗	✗	✗
11	DCAN RTR mask result information (Technical Limitation)		✗	✗	✓	✗
12	DCAN High Speed RX Loss and falsified TX ID		✗	✗	✗	✗
13	DCAN Extended Identifier (Technical Limitation)		✗	✗	✗	✗

No.	Outline		µPD78F0948			µPD780948
		Rev.	V4.0	V5.1	V6.0	V3.0
		Rank Note	E	X, M	H, W	E
14	Timer 5n – Data match Interval timer mode (Technical Limitation)		✗	✓	✓	✓
15	Timer 5n – Data match Square wave output mode (Technical Limitation)		✗	✓	✓	✓
16	Timer 5n – Data match PWM mode (Technical Limitation)		✗	✓	✓	✓
17	Timer 5n – Interrupt (Technical Limitation)		✓	✗	✓	✗
18	Flash memory characteristics (Technical Limitation)		✗	✗	✓	No Flash
19	Flash programming (Technical Limitation)		✗	✓	✓	No Flash

✓ : Not applicable
✗ : applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

No.	Outline		µPD78F0948A			µPD780948A		
		Rev.	V6.0			V4.1		
		Rank Note	all			all		
6	DCAN REDEF Limitation (Technical Limitation)		✗			✗		
7	DCAN SLEEP request (Technical Limitation)		✗			✗		
8	DCAN Initialization of TXA bits (Technical Limitation)		✗			✗		
9	DCAN Sample point Timing, Glitch Detection and Resynchronization (Technical Limitation)		✗			✗		
10	DCAN Resynchronization (Technical Limitation)		✗			✗		
13	DCAN Extended Identifier (Technical Limitation)		✗			✗		

✓ : Not applicable
✗ : applicable

Note: The rank is indicated by the letter appearing at the 5th position from the left in the lot number, marked on each product.

(B) Description of Operating Precautions

No. 1	DCAN The compare state machine for frame reception (Technical Limitation)
	Details The state machine responsible for the comparison of received identifiers with the identifiers in the RAM is started when the first data arrives. When a stuff error is encountered, the frame is interrupted. At that time the compare machine may wait for an additional identifier bit from the bus until the expected data is received from the next receive frame. Then the comparison is executed on mixed data from two frames.

No. 2	DCAN Change from Error Active State to Error Passive State during error frames (Technical Limitation)
	Details The CAN protocol requires a change from Error Active to Error Passive when one error counter (REC or TEC) is greater than 127. The DCAN does not change the status due to uninterrupted transmission of error frames when the counter passes the Error Passive level. Instead it will go into Bus Off State (@ TEC = 255) when the error frames were caused during a transmission of a frame. For error frames caused during reception of a frame the DCAN keeps transmitting active error frames until it can detect the dominant level.

No. 3	DCAN Hard synchronization during all required situations (Technical Limitation)
	Details The DCAN performs the hard synchronization only when the bus is idle as described in the original protocol. It does no hard synchronization when one node sends its start of frame already in the 3rd bit of the Intermission field. The DCAN performs a soft synchronization instead. This may lead to an error during the reception of the frame. This occurs only when the different nodes on the bus have high oscillator tolerances

No. 4	DCAN Hard synchronization instead of soft synchronization (Technical Limitation)
	Details The DCAN performs synchronization similar to a hard synchronization when a dominant to recessive edge is detected in the last time quantum before the Sample point. This may result in a synchronization error during the rest of the frame.

No. 5	DCAN Suspend transmission operation (Technical Limitation)
	Details In case the DCAN is error passive and a transmission is waiting, the transmitter has to wait for suspend transmission time to be passed, before it can transmit any data on the bus. This delay can cause the following reactions a) When another node starts a frame in the third bit of the intermission the DCAN does not synchronize to this frame. This leads to an error during the reception of the frame. In case the DCAN is already Error Passive the data is lost. The DCAN may also send one dominant bit on the bus. It depends on the identifier of the frame that is waiting for transmit in the DCAN b) When another node starts a frame with the first bit of bus idle the DCAN may transmit one dominant bit that can destroy the arbitration process. In addition the next frame to be transmitted may have a wrong identifier.

No. 6	DCAN REDEF Limitation (Technical Limitation)
	Details When the REDEF function is executed for a particular receive message buffer during message reception, unexpected message reception in another receive message buffer can occur. Also a message for a buffer not put into redefinition state may not be received although the acceptance filer criteria is met. For detailed description and workaround, pls. refer to the document EACT-BR-5006-1.0.pdf or later. *Workaround* Issue REDEF function only directly after 'bus idle' was detected. Use RXF and TXF bits in CAN control register CANC for this purpose and disable all interrupt during these operations. Alternatively the regular initialization mode can be used for re-configuration of the message buffer area or when REDEF was used to provide data consistency, this method needs to be replaced by the normal method using DN and MUC bit.
No. 7	DCAN SLEEP request (Technical Limitation)
	Details The DCAN cannot be set to SLEEP or STOP mode when an error frame was last on the bus. After detecting a valid frame this lock is abolished. This behavior has no influence to the CAN protocol on the CAN bus. *Workaround* Set the DCAN in INIT mode and check the state with the INITSTATE bit in the CANES register. Then leave the INIT mode again. After the DCAN has synchronized to the bus (detecting 11 recessive bits) and has detected the idle state (19 recessive bits) a request for SLEEP or STOP will be accepted.

No. 8	DCAN Initialization of TXA bits (Technical Limitation)
	Details Setting INIT in the CANC register does not clear the bits 2 and 3 in TCR register (TXAn). Therefore the first transmit in each buffer can be aborted, depending on the status of TXAn before INIT mode. After RESET TXAn bit is cleared. *Workaround* If TXAn is set after leaving INIT mode, the first transmission for buffer n has to be checked with the TXCn bit. The TXCn bit is valid after TXRQn is cleared by the DCAN. If TXCn is zero the message was not transmitted successfully and has to be requested again.

No. 9	DCAN Sample point Timing, Glitch Detection and Resynchronization (Technical Limitation)
	Details Sample point Timing: The real sample point is before the allowed position. It is not possible to adjust the sample point to the segment change from PHSEG1 (TSEG1) to PHSEG2 (TSEG2). This leads to a reduction of the maximal wire length. Glitch Detection: If during CAN Bus IDLE a glitch is located on the bus in the last two time quanta before the expected sample point location, it could be interpreted as Start of Frame. As a result a Stuff Bit Error will be detected and an ERROR Frame will be transmitted. Resynchronization: If a receiving CAN node recognizes a falling edge in Phase Buffer Segment 2, this segment has to be shortened due to CAN Specification 2.0B. No synchronization is performed when the falling edge is in the last time quanta of PHSEG2 and a dominant bit is next to send. This could happen if the module is in its arbitration phase (transmit mode) or it sends an acknowledge flag (receive mode).

No. 10	DCAN Resynchronization (Technical Limitation)
	Details According to the CAN protocol specification (BOSCH CAN specification, version 2.0, Sept. 1991, part A, chapter 8) a CAN node has to perform a soft-synchronization, when acting as a transmitter sending a dominant bit if a recessive to dominant edge occurs after the sample point within phase segment 2. This scenario is only encountered in case of a disturbance. For this case the soft-synchronization is not performed by the implementations listed below. As a consequence the nominal length of an error frame that follows this disturbance can be extended by the amount of time quanta allocated for the synchronization jump width.

No. 11	DCAN RTR mask result information (Technical Limitation)
	Details Using mask function allows masking the RTR bit, but without storing of the information which RTR was received, in bit 0 of the IDREC1 of the accessed receive buffer. Due to this, it can not be distinguished between data frame and remote frame after reception. The DLC is same in both cases. So it is not known whether new data or just a remote frame arrived.

No. 12	DCAN High speed RX Loss and falsified TX ID (Technical Limitation)
	Details For detailed description and workaround, pls. refer to the document EACT-BR-5004-1.0.pdf or later.

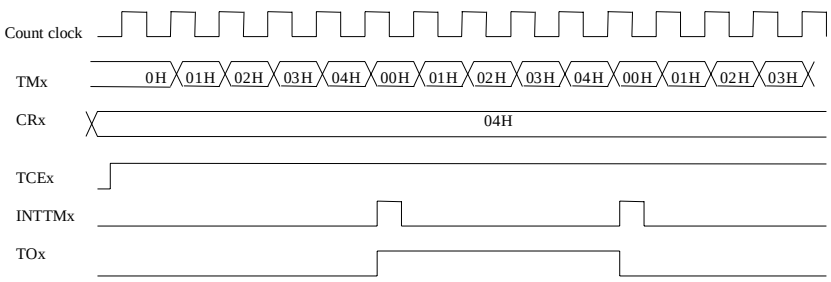
No. 13	DCAN Extended Identifier (Technical Limitation)
	Details and Workaround The DCAN encounters an unexpected behavior with respect to the reception of messages with Extended Identifier. While error-Frames or stuff-Bit-errors occur on the CAN-bus within specific time-slots, the data-contents of messages with same Standard ID-part, but differing within the Extended ID-part, can be mixed, may be lost or wrong stored. For detailed description and possible workarounds pls. refer to the document EACT-BR-5010-1.2 or later.

No. 14	Timer 5n – Data match Interval timer mode (Technical Limitation)

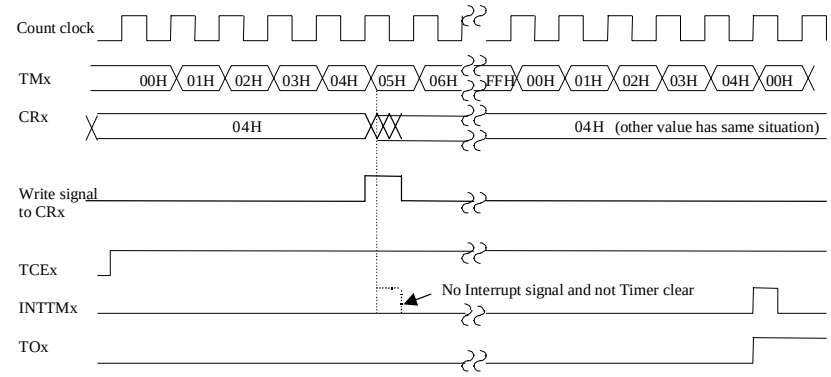
Details

When the compare value is written to the compare register CR5n and the timer register TM5n matches the value of the compare register CR5n, no interrupt INTTM5n will be generated.

In case of operation of Interval timer and Square wave output (at Correct operation)



In case of operation of Interval timer and Square wave output (at Bug operation)



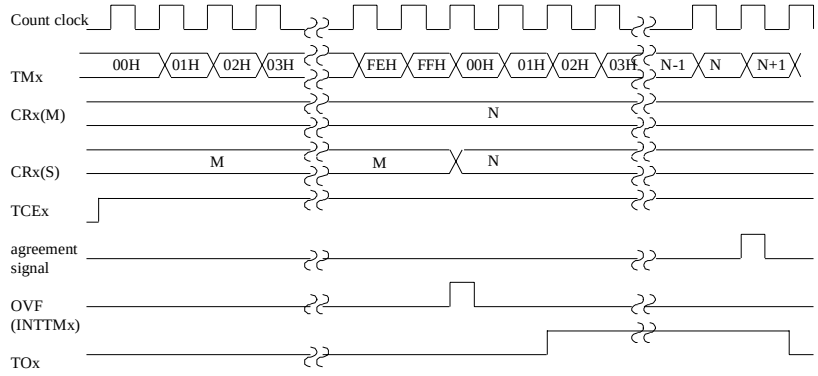
Caution) A.m Timing chart is rough figure.

No. 15	Timer 5n – Data match Square wave output mode (Technical Limitation)

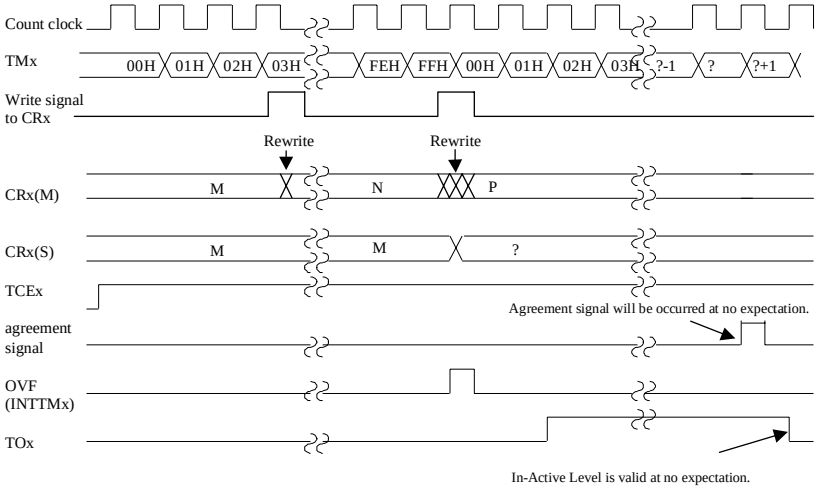
Details

When the compare value is written to the compare register CR5n and the timer register TM5n matches the value of the compare register CR5n, no interrupt INTTM5n will be generated. Additionally, the output flip-flop is not inverted.

In case of operation of PWM output mode (at Correct operation)



In case of operation of PWM output mode (at Bug operation)



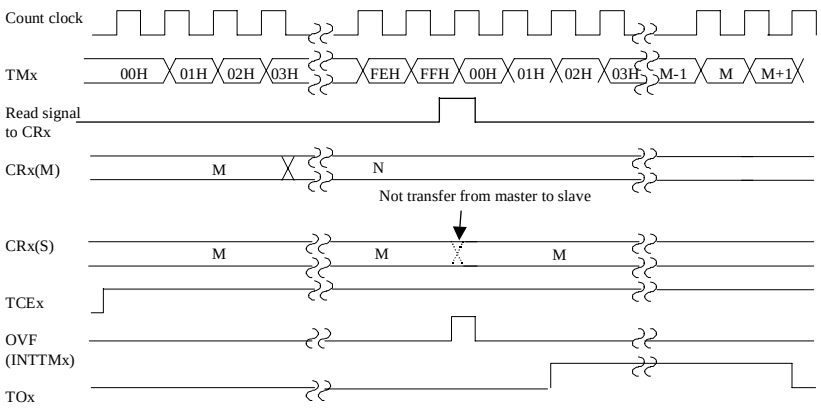
Caution) A.m Timing chart is rough figure.

No. 16	Timer 5n – Data match PWM mode (Technical Limitation)

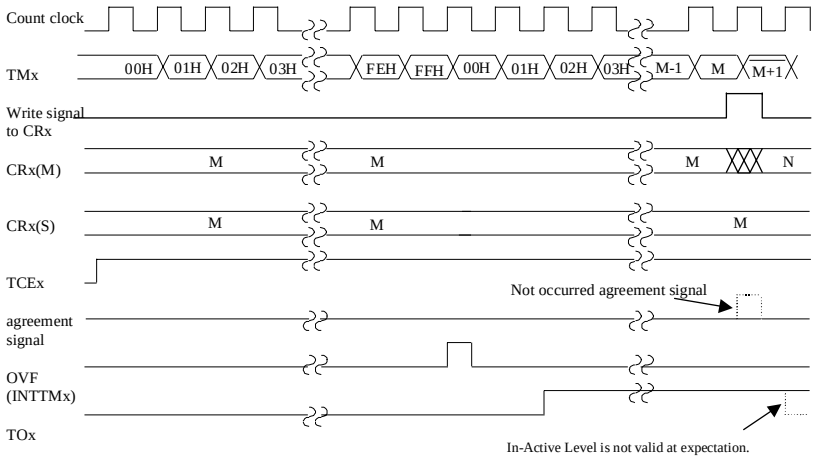
Details

When the compare value is written to the compare register CR5n and the timer register TM5n matches the value of the compare register CR5n, no interrupt INTTM5n will be generated. When the compare value is written or read to/from the compare register CR5n at the time the timer overflows, the PWM output is undefined for one cycle.

In case of operation of PWM output mode (at Bug operation)



In case of operation of PWM output mode (at Bug operation)

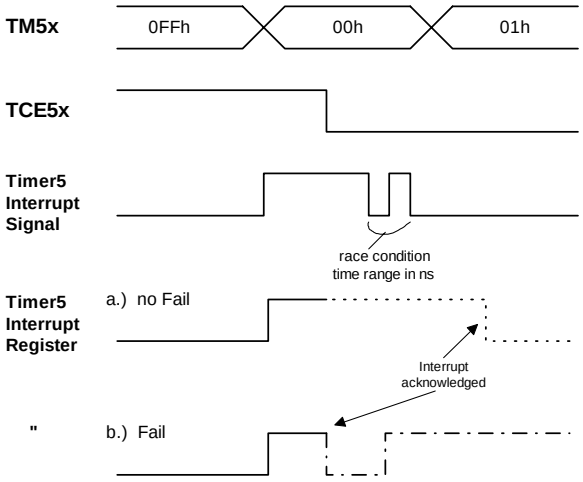


Caution) A.m Timing chart is rough figure.

No. 17	Timer 5n – Interrupt (Technical Limitation)

Details

The Timer5n generates a carry information in the PWM-Mode, if the counter reaches the value 0FFh. This signal is used to generate the interrupt signal. If during that time TCE5n bit is cleared a second interrupt might be generated.
Delays in two depending paths are in a race condition. This occurs depending on process condition and operation condition such as VDD and temperature.



As shown in the diagram above, the second interrupt can only occur if the interrupt is acknowledged, the TCE5x is cleared and the Timer5n has the value 00h after an overrun. This scenario is only feasible if the Timer5n is configured with a slow pre-scaler clock and a short interrupt time.

Workaround

Mask the interrupt before stopping the operation of Timer5n with resetting the register TCE5n. Please see below a few sample code lines:

```
    :
SET1    TMMK5n    ;Mask the interrupt of Timer5n
CLR1    TCE5n     ;Stop operation of Timer5n
CLR1    TMIF5n    ;Clear the interrupt register of Timer5n
CLR1    TMIF5n    ;Clear the interrupt register of Timer5n
CLR1    TMMK5n    ;Clear the mask of the interrupt of Timer5n
    :
```

No. 18	Flash memory characteristics (Technical Limitation)

Details

V4.0 and V5.1 do not satisfy the specification with respect to the number of W/E cycles.

	Number of W/E Cycles	Operating Temperature	Temperature for Rewriting	Data Retention Time
Target specification	20 Times	-40 to +85°C	+10 to +40°C	10 Years
V4.0 and V5.1	5 Times	-40 to +85°C	+10 to +40°C	10 Years
V6.0	20 Times	-40 to +85°C	+10 to +40°C	10 Years

No. 19	Flash programming (Technical Limitation)

Details

The µPD78F0948 V4.0 cannot be programmed via the UART and SIO interface as specified when the flashMaster is used.

Workaround

For programming the µPD78F0948 V4.0 use the SIO interface and supply a device clock of 4MHz (crystal) from the target.

The flashMaster must then be set as follows:

COM port = CSI Ch-0
SIO clock = 100kHz
Target = 8MHz (although target board crystal is 4MHz)

Verification is already done when the displayed message after programming is OK. An additional verification can only achieved by using the programming function with the same HEX file again.

(C) Valid Specification

Item	Date published	Document No.	Document Title
1	April 2003	U16506EE1V0UD00	µPD780948A Subseries Preliminary User's Manual
2	April 2003	U12670EE3V0UD00	µPD780948 Subseries User's Manual

(D) Revision History

Item	Date published	Document No.	Comment
1	July 24, 2003	TPS-LE-OP-F0948A	1st Release
2	January 21, 2005	TPS-LE-OP-F0948A-1	1st Update Items 3 to items 5 added
3	March 7, 2005	TPS-LE-OP-F0948A-2	2nd Update Merging of documents TPS-LE-OP-F0818-1 and TPS-LE-OP-F0948-3 µPD780948 Subseries: Addition of item 13 µPD780948A Subseries: Addition of item 13