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<b>Concerned Products:</b>  IE-780308-R-EM	<b>Customer Notification</b>		Date: July 2 <sup>nd</sup> , 1999
			NEC-Electronics (Europe) GmbH EAD – Technical Product Support
	<b>Bug Report</b>		Source Doc: SBG-T-0819, SBG-T-1655
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Date of initial issue:	Nov. 18th, 98	Doc. No.:	TPS-LE-B-0T003
1 <sup>st</sup> revision	: Jul. 2 <sup>nd</sup> , 99	Doc. No.:	TPS-LE-B-0T003-1
2 <sup>nd</sup> revision	:	Doc. No.:	TPS-LE

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**(A) BUG LIST (1/2)**

Bug No.	Outline	IE-780308-R-EM				
		V2.00 Code "A"	V2.10 Code "B"	V2.21 Code "C"	V2.22 Code "D"	V2.? Code "E"
1	Port 60 to 63	✎	✓	✓	✓	✓
2	Power supply at user voltage	⚡	✎	✓	✓	✓
3	Interrupt of serial interface channel 3	⚡	⚡	✎	✓	✓
4	Emulation bug after reset release	⚡	⚡	⚡	✎	✓
5	TCL4 register read/write	⚡	⚡	⚡	⚡	⚡

- ✓: No problem
- ✎: Bug (will be corrected by next version upgrade)
- ⚡: Bug (restriction, not corrected by version upgrade)

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**(B) BUG DESCRIPTION**

Bug No.	Outline	Description													
1	Port 60 to 63	The low voltage power supply is connected with the emulation circuit of the ports P60 to P63. Due to this the high level output voltage of P60 to P63 does not rise above the level of the low voltage power supply.													
2	Power supply at user voltage	The power supply via user voltage from the target hardware can cause a system latch-up.													
3	Interrupt of serial interface channel 3	The transfer termination interrupt (INTCSI3) of the serial interface channel 3 can occur abnormally.													
4	Emulation bug after reset release	The P24, P24, P70 and P71 input data values will be undefined from the period immediately after reset release to the initialisation of PM2 and PM7 during the emulation of the $\mu$ PD7805x series and the $\mu$ PD78005x series.													
5	TCL4 register read/write	<p>This product has a restriction related to the read/write operation of the timer clock selection register TCL4 during the emulation of the <math>\mu</math>PD78030x series. As indicated in the table below, only the user program write operation is performed normally</p> <table border="1"> <thead> <tr> <th colspan="2">TCL4 register operations</th> <th>Result</th> </tr> </thead> <tbody> <tr> <td rowspan="2">SFR window</td> <td>read</td> <td>Undefined value</td> </tr> <tr> <td>write</td> <td>Undefined value</td> </tr> <tr> <td rowspan="2">User program</td> <td>read</td> <td>Undefined value</td> </tr> <tr> <td>write</td> <td>Write to TCL4 (normal operation)</td> </tr> </tbody> </table>	TCL4 register operations		Result	SFR window	read	Undefined value	write	Undefined value	User program	read	Undefined value	write	Write to TCL4 (normal operation)
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SFR window	read	Undefined value													
	write	Undefined value													
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