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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A714A/E	Rev.	1.00
Title	Omitted Description in Passages on Conditions for Clearing the TEND, TDRE, and RDRF Bits in the SSU Module		Information Category	Technical Notification		
Applicable Product	SH7147 Series products	Lot No. All lots	Reference Document	See below.		

We would like to inform you of omissions in the descriptions of conditions for clearing the TEND, TDRE, and RDRF bits in the SSU module of applicable products.

[Corrections]

14.3.5 SS Status Register (SSSR)

[Before change]

Bit	Bit Name	Initial Value	R/W	Description
3	TEND	0	R/W	Transmit End [Setting conditions] • When the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is cleared to 0 and the TDRE bit is set to 1 • After the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is set to 1 and the TDRE bit is set to 1 [Clearing conditions] • When writing 0 after reading TEND = 1 • When writing data to SSTDR
2	TDRE	1	R/W	Transmit Data Empty Indicates whether or not SSTDR contains transmit data. [Setting conditions] • When the TE bit in SSER is 0 • When data is transferred from SSTDR to SSTRSR and SSTDR is ready to be written to. [Clearing conditions] • When writing 0 after reading TDRE = 1 • When writing data to SSTDR with TE = 1 • When the DTC is activated by an SSTXI interrupt and transmit data is written to SSTDR while the DISEL bit in MRB of the DTC is 0

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Bit	Bit Name	Initial Value	R/W	Description
1	RDRF	0	R/W	Receive Data Register Full Indicates whether or not SSRDR contains receive data. [Setting condition] • When receive data is transferred from SSTRSR to SSRDR after successful serial data reception [Clearing conditions] • When writing 0 after reading RDRF = 1 • When reading receive data from SSRDR • When the DTC is activated by an SSRXI interrupt and receive data is read into SSRDR while the DISEL bit in MRB of the DTC is 0

[After change]

Bit	Bit Name	Initial Value	R/W	Description
3	TEND	0	R/W	Transmit End [Setting conditions] When the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is cleared to 0 and the TDRE bit is set to 1 After the last bit of transmit data is transmitted while the TENDSTS bit in SSCR2 is set to 1 and the TDRE bit is set to 1 [Clearing conditions] When writing 0 after reading TEND = 1 When writing data to SSTDR wIth FCLRM = 1 When the DTC is activated by an SSTXI interrupt and transmit data is written to SSTDR while the DISEL bit in MRB of the DTC is 0 (unless the transfer counter value of the DTC is H'0000)*
2	TDRE	1	R/W	Transmit Data Empty Indicates whether or not SSTDR contains transmit data. [Setting conditions] When the TE bit in SSER is 0 When data is transferred from SSTDR to SSTRSR and SSTDR is ready to be written to. [Clearing conditions] When writing 0 after reading TDRE = 1 When writing data to SSTDR with TE = 1 and FCLRM = 1 When the DTC is activated by an SSTXI interrupt and transmit data is written to SSTDR while the DISEL bit in MRB of the DTC is 0 (unless the transfer counter value of the DTC is H'0000)*

Bit	Bit Name	Initial Value	R/W	Description
1	RDRF	0	R/W	Receive Data Register Full Indicates whether or not SSRDR contains receive data. [Setting condition] When receive data is transferred from SSTRSR to SSRDR after successful serial data reception [Clearing conditions] When writing 0 after reading RDRF = 1 When reading receive data from SSRDR with FCLRM = 1 When the DTC is activated by an SSRXI interrupt and receive data is read into SSRDR while the DISEL bit in MRB of the DTC is 0 (unless the transfer counter value of the DTC is H'0000)*

Note: * When using the DTC transfer, be sure to set the FCLRM bit to 0.

[Before change]

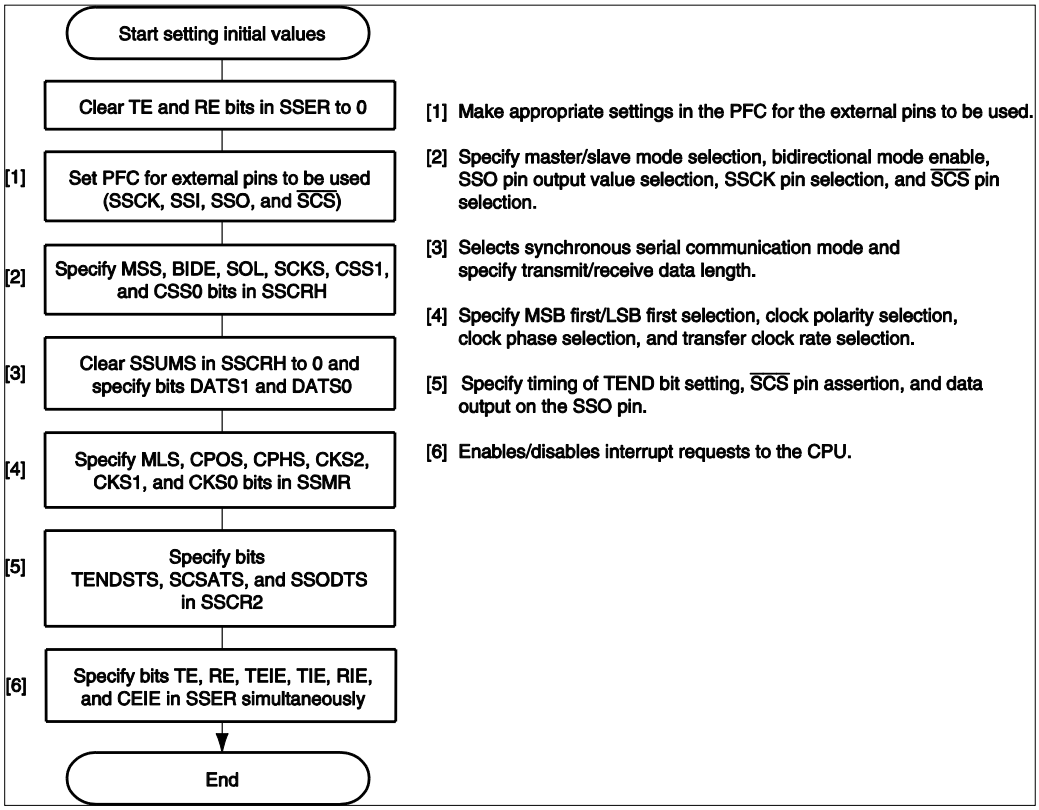

Figure 14.4 Example of Initial Settings in synchronous Serial Communication Mode

[After change]

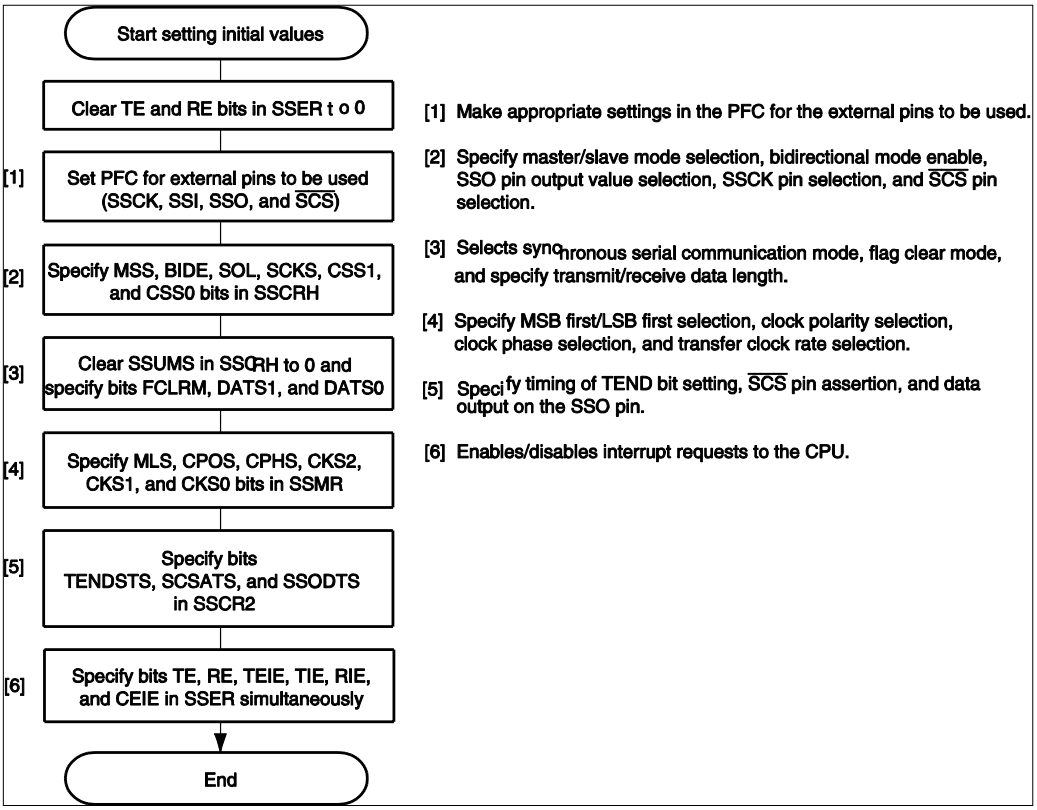

Figure 14.4 Example of Initial Settings in synchronous Serial Communication Mode

[Before change]

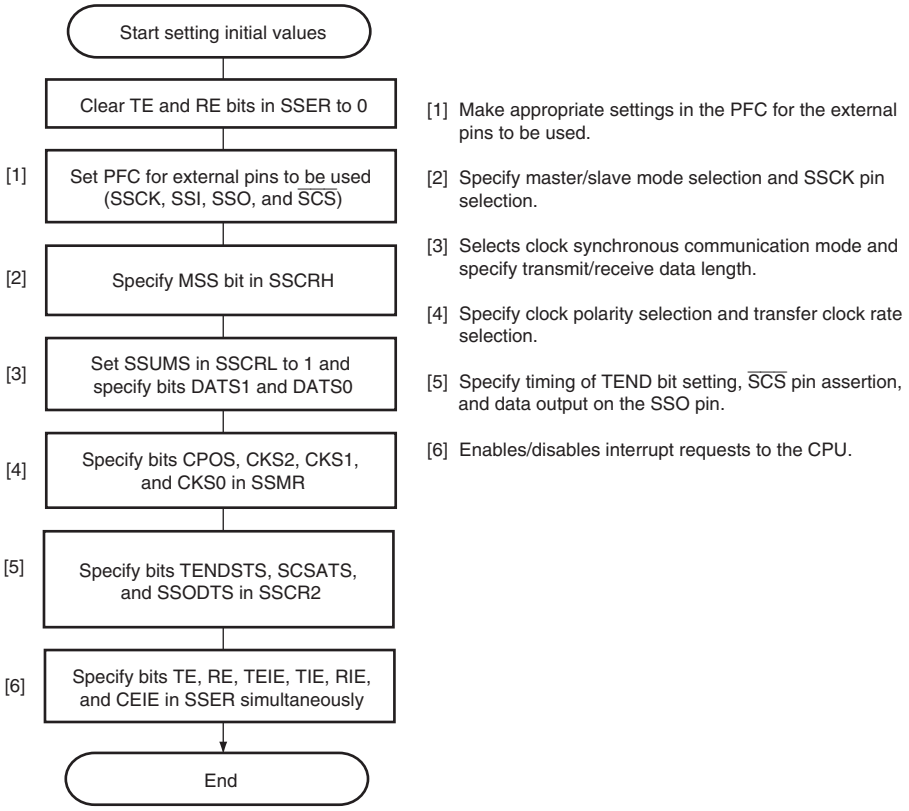

Figure 14.12 Example of Initial Settings in Clock Synchronous Communication Mode

[After change]

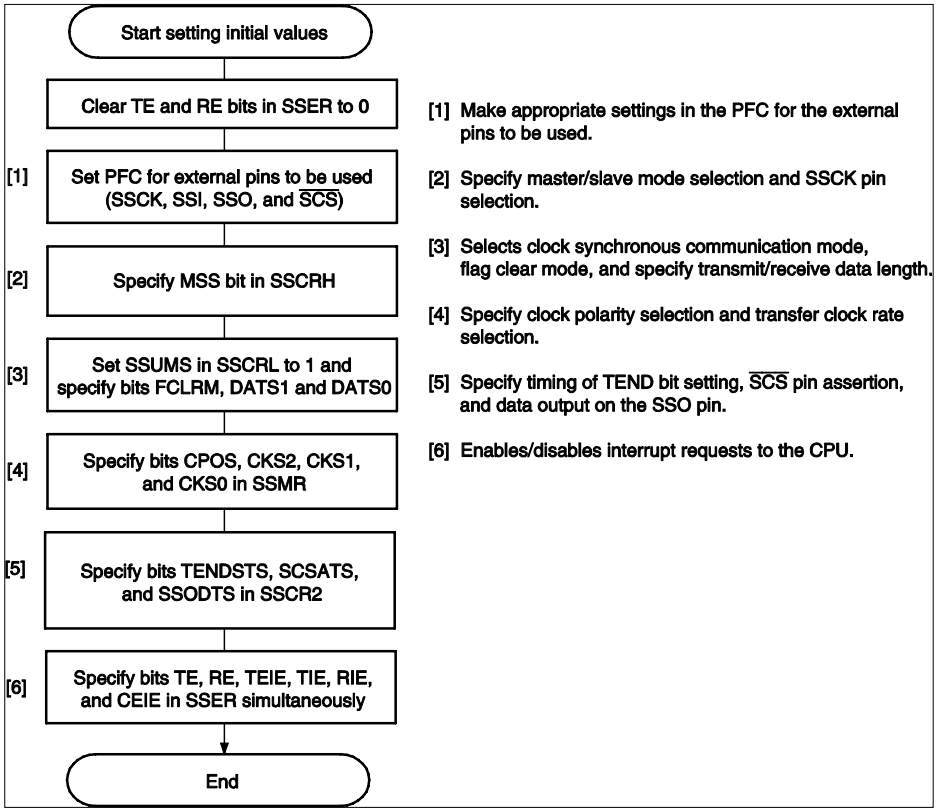

Figure 14.12 Example of Initial Settings in Clock Synchronous Communication Mode

[Related Manual]

Series	Group	Related Manual	Rev.	Document Number
SH7147	SH7147	SH7147 Group Hardware Manual	3.00	REJ09B0230-0300