Date: Mar. 24, 2017

# RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

| Product Category | System LSI | Document No. | TN-RIN-A023A/E | Rev. | 1.00 |
|---|---|---|---|---|---|
| Title | Notification of R-IN32M4-CL2 User's Manual (Rev.1.01 to Rev.1.02) Revised contents: Corrections and new functions | | Information Category | Technical Notification | |
| Applicable Product | See following | Lot No. / All lots | Reference Document | R-IN32M4-CL2 Series User's Manual: R9J03G019GBG Rev.1.02 (R18UZ0033EJ0102) | |

R-IN32M4-CL2 User's Manual Rev. 1.02 (R18UZ0033EJ0102) has been released on Renesas website. This technical update follows revision 1.01 and includes the entirety of revised items. For details, refer to "2. Documentation Updates" given below.

## 1 Applicable Product

| Product Type | Model Marking | Product Code |
|---|---|---|
| R-IN32M4-CL2 | R9J03G019 | R9J03G019GBG |

## 2 Documentation Updates

| No | Applicable Item (Rev. 2.01 Section) | Applicable Page (Rev. 2.01) | Contents |
|---|---|---|---|
| 1 | 2.1.2 Ethernet Pins | 13 | Error correction |
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| 7 | 5. Peripheral Modules | 60 | Expression alignment |
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| 9 | 6.1.3 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD) | 63 | Complement |
| 10 | 7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE,EXTPFCE) | 88 | Complement |
| 11 | 8.4 DC Characteristics (Table 8.7) | 119 | Error correction |

## No.1 2.1.2 Ethernet Pins

## Nonexistent Pins (for thermal sensor and regulator) deleted

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**[2.1.2 Ethernet Pins]**

| Function Name | Pin Name | I/O | Description | Active | Level during Reset |
|---|---|---|---|---|---|
| REF_FILT | – | I/O | Copper media reference filter pin. | – | – |
| REF_REXT | – | I/O | Copper media reference external pin. | – | – |
| THERMDA | – | I/O | Thermal diode anode. | – | – |
| THERMDC_VSS | – | I/O | Thermal diode cathode connected to device ground. Temperature sensor must be chosen accordingly. | – | – |
| VDD1 | – | – | 1.0 V internal power supply | – | – |
| VDD1A | – | – | 1.0 V analog power requiring additional PCB power supply filtering | – | – |
| VDD25A | – | – | 2.5 V general analog power supply | – | – |
| VDD33_GPHY | – | – | 3.3 V general I/O power supply | – | – |

| Function Name | Pin Name | I/O | Description | Active | Level during Reset |
|---|---|---|---|---|---|
| PHY0_LED0 | – | Output | GbE-PHY LED0_PHY0 output signal | Low | High |
| PHY1_LED0 | – | Output | GbE-PHY LED0_PHY1 output signal | Low | High |
| ETHSWSYNCOUT | P24 | Output | Ether switch event output | High | Hi-Z (High) |
| VDDREG_33_10 | – | – | 3.3 V power for 1.0V regulator[Note] | – | – |
| VDDREG_33_25 | – | – | 3.3 V power for 2.5V regulator[Note] | – | – |
| REG_EN_10 | – | Input | 1.0 V Regulator enable[Note] | – | – |
| REG_EN_25 | – | Input | 2.5 V Regulator enable[Note] | – | – |
| ERRIN_10 | – | – | Off-chip compensation for regulator[Note] | – | – |
| ERROUT_10 | – | – | Off-chip compensation for regulator[Note] | – | – |
| ERRNEG_10 | – | – | Off-chip compensation for regulator[Note] | – | – |
| ERRIN_25 | – | – | Off-chip compensation for regulator[Note] | – | – |
| ERROUT_25 | – | – | Off-chip compensation for regulator[Note] | – | – |
| ERRNEG_25 | – | – | Off-chip compensation for regulator[Note] | – | – |
| REG_OUT_10 | – | – | 1.0 V Regulator output[Note] | – | – |
| REG_OUT_25 | – | – | 2.5 V Regulator output[Note] | – | – |

**Note. This product does not support an internal regulator. These pins should be handled appropriately when they are not in use.**

**For details, see section 2.5.2 Ethernet Pins.**

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**[2.1.2 Ethernet Pins]**

| Function Name | Pin Name | I/O | Description | Active | Level during Reset |
|---|---|---|---|---|---|
| REF_FILT | – | I/O | Copper media reference filter pin. | – | – |
| REF_REXT | – | I/O | Copper media reference external pin. | – | – |
| VDD1 | – | – | 1.0 V internal power supply | – | – |
| VDD1A | – | – | 1.0 V analog power requiring additional PCB power supply filtering | – | – |
| VDD25A | – | – | 2.5 V general analog power supply | – | – |
| VDD33_GPHY | – | – | 3.3 V general I/O power supply | – | – |
| PHY0_LED0 | – | Output | GbE-PHY LED0_PHY0 output signal | Low | High |
| PHY1_LED0 | – | Output | GbE-PHY LED0_PHY1 output signal | Low | High |
| ETHSWSYNCOUT | P24 | Output | Ether switch event output | High | Hi-Z (High) |

## No.2 2.1.11 CC-Link Pins (Intelligent Device Station)

**Feature of the CCM_MDIN0-3 signals modified**

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>26</td><td>[2.1.11 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Function Name</th><th>Pin Name</th><th>I/O</th><th>Description</th><th>Active</th><th>Level during Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>P20</td><td>Output</td><td>Link error LED control output</td><td>Low</td><td>Hi-Z (High)</td></tr>
<tr><td>CCM_ERRZ</td><td>P21</td><td>Output</td><td>Error LED control output</td><td></td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>P26</td><td>Output</td><td>Run LED control output</td><td></td><td></td></tr>
<tr><td>CCM_MDIN0-<br>CCM_MDIN3</td><td>P62-P65</td><td>Input</td><td>Mode setting switch input</td><td>–</td><td></td></tr>
<tr><td>CCM_SNIN0-<br>CCM_SNIN7</td><td>P70-P77</td><td>Input</td><td>Station no. setting switch input</td><td></td><td></td></tr>
</table></td><td>25</td><td>[2.1.11 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Function Name</th><th>Pin Name</th><th>I/O</th><th>Description</th><th>Active</th><th>Level during Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>P20</td><td>Output</td><td>Link error LED control output</td><td>Low</td><td>Hi-Z (High)</td></tr>
<tr><td>CCM_ERRZ</td><td>P21</td><td>Output</td><td>Error LED control output</td><td></td><td></td></tr>
<tr><td>CCM_RUNZ</td><td>P26</td><td>Output</td><td>Run LED control output</td><td></td><td></td></tr>
<tr><td>CCM_MDIN0-<br>CCM_MDIN3</td><td>P62-P65</td><td>Input</td><td>Transfer rate and mode setting switch input</td><td>–</td><td></td></tr>
<tr><td>CCM_SNIN0-<br>CCM_SNIN7</td><td>P70-P77</td><td>Input</td><td>Station no. setting switch input</td><td></td><td></td></tr>
</table></td></tr>
</table>

## No.3 2.1.16 System Pins

**Function of PONRZ modified**

<table>
<tr><th colspan="2">V1.01</th><th colspan="2">V1.02</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>28</td><td>[2.1.13 System Pins]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>PONRZ</td><td>I</td><td>Internal RAM power on reset input</td><td>Low</td><td>-</td></tr>
</table></td><td>27</td><td>[2.1.13 System Pins]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Active</th><th>Level during & after Reset</th></tr>
<tr><td>PONRZ</td><td>I</td><td>Power on reset input</td><td>Low</td><td>-</td></tr>
</table></td></tr>
</table>

## No.4 2.5.2 Ethernet Pins

### Nonexistent pins (for thermal sensor) deleted

**V1.01**

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**[2.5.2 Ethernet Pins]**

| Pin Name | I/O | Interface | Recommended Connection when Not in Use |
|---|---|---|---|
| REF_FILT | I/O | Copper media reference filter pin. | Connect the pin to GND via an external 1uF capacitor. Handle the pin in this way at all times. |
| REF_REXT | I/O | Copper media reference external pin. | Connect the pin to GND via an external 2.0k Ohm (1%) resistor. Handle the pin in this way at all times. |
| THERMDA | I/O | Thermal diode anode. | Open |
| THERMDC_VSS | I/O | Thermal diode cathode connected to device ground. Temperature sensor must be chosen accordingly. | Open |
| VDD1 | – | 1.0-V internal power supply | Connect to VDD (1.0V) |
| VDD1A | – | 1.0-V analog power requiring additional PCB power supply filtering | Connect to VDD (1.0V) |
| VDD25A | – | 2.5-V general analog power supply | Connect to VDD (2.5V) |
| VDD33_GPHY | – | 3.3-V general I/O power supply | Connect to VDD (3.3V) |
| PHY0_LED0 | Output | GbE-PHY LED0_PHY0 output signal Output buffer (3.3V) 3m A | Open |
| PHY1_LED0 | Output | GbE-PHY LED0_PHY1 output signal Output buffer (3.3V) 3m A | Open |

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**[2.5.2 Ethernet Pins]**

| Pin Name | I/O | Interface | Recommended Connection when Not in Use |
|---|---|---|---|
| REF_FILT | I/O | Copper media reference filter pin. | Connect the pin to GND via an external 1uF capacitor. Handle the pin in this way at all times. |
| REF_REXT | I/O | Copper media reference external pin. | Connect the pin to GND via an external 2.0 kΩ (1%) resistor. Handle the pin in this way at all times. |
| VDD1 | – | 1.0 V internal power supply | Connect to VDD (1.0V) |
| VDD1A | – | 1.0 V analog power requiring additional PCB power supply filtering | Connect to VDD (1.0V) |
| VDD25A | – | 2.5 V general analog power supply | Connect to VDD (2.5V) |
| VDD33_GPHY | – | 3.3 V general I/O power supply | Connection to VDD (3.3V) |
| PHY0_LED0 | Output | GbE-PHY LED0_PHY0 output signal Output buffer (3.3V) 3m A | Open |
| PHY1_LED0 | Output | GbE-PHY LED0_PHY1 output signal Output buffer (3.3V) 3m A | Open |

## No.5 4.2 List of Interrupts

### Exception No.54 INTETHSW: Interrupt source name changed

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**[4.2 List of Interrupts]**

[Table 4.1 List of Interrupts]

(2/4)

| Exception No. | Name | Interrupt Source | Connected to | | | | |
|---|---|---|---|---|---|---|---|
| | | | NVIC | HW-RTOS | DMAC | Real Time Port | Timer TAUJ2 /TAUD |
| 54 | INTETHSW | Ether SWITCH interrupt | ○ | ○ | ○ | ○ | ○ |

**V1.02**

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**[4.2 List of Interrupts]**

[Table 4.1 List of Interrupts]

(2/4)

| Exception No. | Name | Interrupt Source | Connected to | | | | |
|---|---|---|---|---|---|---|---|
| | | | NVIC | HW-RTOS | DMAC | Real Time Port | Timer TAUJ2 /TAUD |
| 54 | INTETHSW | Ether SWITCH Timer interrupt <R> | ○ | ○ | ○ | ○ | ○ |

## No.6 4.2 List of Interrupts

### Table 4.1, ECC error interrupts added

**V1.01**

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**[4.2 List of Interrupts]**
[Table 4.1 List of Interrupts (4/4)]

| Exception No. | Name | Interrupt Source | Connected to | | | | |
|---|---|---|---|---|---|---|---|
| | | | NVIC | HW-RTOS | DMAC | Real Time Port | Timer TAUJ2 /TAUD |
| 111 | INTLED0PHY0 | Gigabit Ethernet PHY LED0_PHY0 input interrupt | ○ | ○ | ○ | ○ | ○ |
| 112 | INTLED0PHY1 | Gigabit Ethernet PHY LED0_PHY1 input interrupt | ○ | ○ | ○ | ○ | ○ |
| 113 | – | Reserved | – | – | – | – | – |
| 114 | – | Reserved | – | – | – | – | – |
| 115 | – | Reserved | – | – | – | – | – |
| 116 | – | Reserved | – | – | – | – | – |
| 117 | – | Reserved | – | – | – | – | – |
| 118 | – | Reserved | – | – | – | – | – |
| 119 | – | Reserved | – | – | – | – | – |
| 120 | – | Reserved | – | – | – | – | – |
| 121 | – | Reserved | – | – | – | – | – |
| 122 | – | Reserved | – | – | – | – | – |

**V1.02**

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**[4.2 List of Interrupts]**
[Table 4.1 List of Interrupts (4/4)]

| Exception No. | Name | Interrupt Source | Connected to | | | | |
|---|---|---|---|---|---|---|---|
| | | | NVIC | HW-RTOS | DMAC | Real Time Port | Timer TAUJ2 /TAUD |
| 111 | INTLED0PHY0 | Gigabit Ethernet PHY LED0_PHY0 input interrupt | ✓ | ✓ | ✓ | ✓ | ✓ |
| 112 | INTLED0PHY1 | Gigabit Ethernet PHY LED0_PHY1 input interrupt | ✓ | ✓ | ✓ | ✓ | ✓ |
| 113 | – | Reserved | – | – | – | – | – |
| 114 | – | Reserved | – | – | – | – | – |
| 115 | IRAMECCSEC | Internal instruction RAM 1-bit ECC error correction interrupt | ✓ | – | – | – | – |
| 116 | DRAMECCSEC | Data RAM 1-bit ECC error correction interrupt | ✓ | – | – | – | – |
| 117 | BRAMECCSEC | Buffer RAM 1-bit ECC error correction interrupt | ✓ | – | – | – | – |
| 118 | IRAMECCDED | Internal instruction RAM 2-bit ECC error detection interrupt | ✓ | – | – | – | – |
| 119 | DRAMECCDED | Data RAM 2-bit ECC error detection interrupt | ✓ | – | – | – | – |
| 120 | BRAMECCDED | Buffer RAM 2-bit ECC error detection interrupt | ✓ | – | – | – | – |
| 121 | – | Reserved | – | – | – | – | – |
| 122 | – | Reserved | – | – | – | – | – |

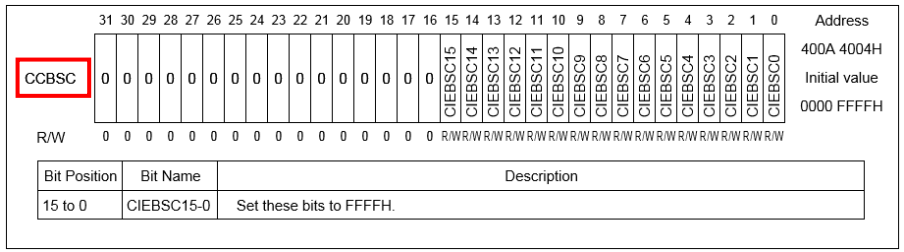
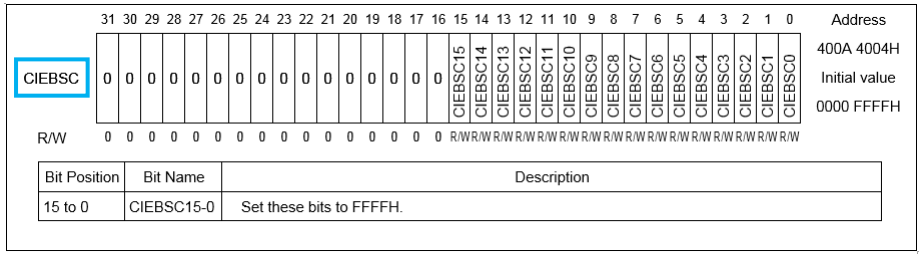
## No.7 5. Peripheral Modules

### Notation of peripheral modules unified to that of User's Manual (Peripheral Modules)

| V1.01 | | V1.02 | |
|---|---|---|---|
| Page | Description | Page | Description |
| 61 | **[5. Peripheral Modules]**<br><br>● Clock function<br>● CPU<br>● Bus structure<br>● Boot procedure<br>● Hardware real-time OS<br>● Gigabit Ethernet PHY<br>● Gigabit Ethernet MAC<br>● Ethernet switch<br>● Asynchronous SRAM memory controller (ROM/RAM)<br>● Synchronous burst access memory controller<br>● External MCU interface<br>● Serial flash ROM memory controller<br>● DMA function<br>● 32-bit timer array unit (TAUJ2)<br>● 16-bit timer array unit (TAUD)<br>● Motor control (TAPA/PIC)<br>● Window watchdog timer A (WDTA)<br>● Asynchronous serial interface J (UARTJ)<br>● Clocked serial interface H (CSIH)<br>● $I^2C$ bus (IICB)<br>● CAN controller (FCN)<br>● 10-bit A/D converter<br>● CC-Link interface<br>● Other interface control<br>● Debugging | 60 | **[5. Peripheral Modules]**<br><br>● Clocks and resets<br>● CPU and internal RAM<br>● Bus structure<br>● Boot procedure<br>● Hardware real-time OS<br>● Gigabit Ethernet PHY<br>● Gigabit Ethernet MAC<br>● Ethernet switch<br>● Asynchronous SRAM memory controller (ROM/RAM)<br>● Synchronous burst access memory controller<br>● External MCU interface<br>● Serial flash ROM memory controller<br>● DMA function<br>● 32-bit timer array unit (TAUJ2)<br>● 16-bit timer array unit (TAUD)<br>● Motor control (TAPA/PIC)<br>● Window watchdog timer A (WDTA)<br>● Asynchronous serial interface J (UARTJ)<br>● Clocked serial interface H (CSIH)<br>● $I^2C$ bus (IICB)<br>● CAN controller (FCN)<br>● 10-bit A/D converter<br>● CC-Link interface<br>● System registers (APB peripheral registers area)<br>● Debugging |

## No.8 6.1.1 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC)

**Regitser symbol in the bit map corrected**

| V1.01 | | V1.02 | |
|---|---|---|---|
| Page | Description | Page | Description |
| 63 | **[6.1.1 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC)]**<br>  <br><br>Bit Position \| Bit Name \| Description<br>15 to 0 \| CIEBSC15-0 \| Set these bits to FFFFH. | 62 | **[6.1.1 CC-Link IE Field (Intelligent Device Station) Bus Size Control Register (CIEBSC)]**<br>  <br><br>Bit Position \| Bit Name \| Description<br>15 to 0 \| CIEBSC15-0 \| Set these bits to FFFFH. |

## No.9 6.1.3 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)

**Reference for the relate registers added**

| V1.01 | | V1.02 | |
|---|---|---|---|
| Page | Description | Page | Description |
| 64 | **[6.1.3 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)]**<br><br>The CIECLKGTD register is used to temporarily stop supply of the bus clock signal. This is to prevent the generation of a clock glitch when switching the bus clock signal from the CC-Link IE field network. Writing 1 to the effective bit of this register stops supply of the clock signal and writing 0 to it causes supply to resume.<br>Before making the setting in the SRAMBRSEL register to switch between the settings to enable the SDRAM bus path from the system bus (AHB) and to enable the SRAM bus path from an external MCU, be sure to use this register to stop the bus clock signal.<br><br>[0: CIECLKGTD]<br>This bit stops supply of the bus clock signal in the CC-Link IE field network.<br>0: Operating<br>1: Stopped | 63 | **[6.1.3 CC-Link IE Field (Intelligent Device Station) Clock Gate Register (CIECLKGTD)]**<br><br>The CIECLKGTD register is used to temporarily stop supply of the bus clock signal. This is to prevent the generation of a clock glitch when switching the bus clock signal from the CC-Link IE Field. Writing 1 to the effective bit of this register stops supply of the clock signal and writing 0 to it causes supply to resume.<br>Before making the setting in the SRAM Bridge Select Register (SRAMBRSEL) to switch between the settings to enable the SRAM bus path from the system bus (AHB) and to enable the SRAM bus path from an external MCU, be sure to use this register to stop the bus clock signal. For details, see section 25.13, SRAM Bridge Select Register (SRAMBRSEL), in the R-IN32M4-CL2 User's Manual: Peripheral Modules.<br><br>[0 : CIECLKGTD]<br>This bit stops supply of the bus clock signal in the CC-Link IE Field.<br>0: Operating<br>1: Stopped |

## No.10 7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE, EXTPFCE)

**Erroneously omitted register EXTPFC was added to notes 1 and 2.**

| V1.01 | | V1.02 | |
|---|---|---|---|
| Page | Description | Page | Description |
| 90 | **[7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE, EXTPFCE)]**<br><br>**Notes To use multiplexed function 1 or 3, the corresponding bit in**<br>**1. the PFC or RPFC register must be set to 0.**<br>**2. To use multiplexed function 2 or 4, the corresponding bit in the PFC or RPFC register must be set to 1.** | 88 | **[7.3.5 Port Function Control Expansion Registers (PFCE, RPFCE, EXTPFCE)]**<br><br>**Notes To use multiplexed function 1 or 3, the corresponding bit in the**<br>**1. PFC, RPFC, or EXTPFC register must be set to 0.**<br>**2. To use multiplexed function 2 or 4, the corresponding bit in the PFC, RPFC, or EXTPFC register must be set to 1.** |

## No.11 8.4 DC Characteristics

**Table 8.7, Symbol for the high-level output voltage modified**

| V1.01 | | V1.02 | |
|---|---|---|---|
| Page | Description | Page | Description |
| 121 | **[8.4 DC Characteristics]**<br>[Table 8.7 DC Characteristics (VDD = 3.3±0.165V, TA = - 40 to +85ºC) (2/2)] | 119 | **[8.4 DC Characteristics]**<br>[Table 8.7 DC Characteristics (VDD = 3.3±0.165V, TA = - 40 to +85ºC) (2/2)] |

V1.01

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-level output current (3.3 V buffer) | $I_{OL}$ | $V_{OL}$ = 0.4V | 6 mA type | 6.0 | – | – | mA |
| | | | 12 mA type | 12.0 | – | – | mA |
| Low-level output current (5V-tolerant buffer) | $I_{OL}$ | $V_{OL}$ = 0.4V | 4 mA type | 4.0 | – | – | mA |
| High-level output current (3.3-V buffer) | $I_{OH}$ | $V_{OH}$ = 2.4V | 6 mA type | - 6.0 | – | – | mA |
| | | | 12 mA type | - 12.0 | – | – | mA |
| High-level output current (5V-tolerant buffer) | $I_{OH}$ | $V_{OH}$ = 2.4V | 4 mA type | - 4.0 | – | – | mA |
| Low-level output current | $V_{OL}$ | $I_{OL}$ = 0mA | 3.3V buffer | – | – | 0.1 | V |
| | | | 5V-Tolerant buffer | – | – | 0.1 | V |
| High-level output current | $V_{OH}$ | $I_{OL}$ = 0mA | 3.3V buffer | $V_{DD}$ - 0.1 | – | – | V |
| | | | 5V-Tolerant buffer | $V_{DD}$ - 0.1 | – | – | V |

V1.02

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-level output current (3.3 V buffer) | $I_{OL}$ | $V_{OL}$ = 0.4V | 6 mA type | 6.0 | – | – | mA |
| | | | 12 mA type | 12.0 | – | – | mA |
| Low-level output current (5V-tolerant buffer) | $I_{OL}$ | $V_{OL}$ = 0.4V | 4 mA type | 4.0 | – | – | mA |
| High-level output current (3.3-V buffer) | $I_{OH}$ | $V_{OH}$ = 2.4V | 6 mA type | - 6.0 | – | – | mA |
| | | | 12 mA type | - 12.0 | – | – | mA |
| High-level output current (5V-tolerant buffer) | $I_{OH}$ | $V_{OH}$ = 2.4V | 4 mA type | - 4.0 | – | – | mA |
| Low-level output current | $V_{OL}$ | $I_{OL}$ = 0mA | 3.3V buffer | – | – | 0.1 | V |
| | | | 5V-tolerant buffer | – | – | 0.1 | V |
| High-level output current | $V_{OH}$ | $I_{OH}$ = 0mA | 3.3V buffer | $V_{DD}$ - 0.1 | – | – | V |
| | | | 5V-tolerant buffer | $V_{DD}$ - 0.1 | – | – | V |