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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	System LSI	Document No.	TN-RIN-A020A/E	Rev.	1.00
Title	Notification of R-IN32M3 Series Datasheet: LSI for Industrial Ethernet (Rev.4.00 to Rev.4.01) Revised contents: Corrections and new functions		Information Category	Technical Notification	
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series Datasheet: LSI for Industrial Ethernet Rev. 4.01 (R18DS0008EJ0401)	

R-IN32M3 Series Datasheet: Industrial Ethernet Rev. 4.01 (R18DS0008EJ0401) has been released on Renesas website. This technical update follows revision 4.00 and includes the entirety of revised items. For details, refer to "2. Documentation Updates" given below.

1 Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
	MC-10287BF1	MC-10287BF1-HN4-A
		MC-10287BF1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A
	D60510BF1	UPD60510BF1-HN4-A
		UPD60510BF1-HN4-M1-A

2 Documentation Updates

No	Applicable Item (Rev. 4.01 Section)	Applicable Page (Rev. 4.01)	Contents
1	2.3.15 CC-Link Pins (Intelligent Device Station)	30	Complement
2	3.14.1(1) External MCU Interface	58	Complement
3	3.14.1(2) AHB master port function	59	Expression alignment
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11	3.19.1 Features	64	New function
12	3.20.1 Features	65	New function
13	4.4 DC Characteristics (Table 4.6)	71	Error correction
14	4.4 DC Characteristics (Table 4.7)	71	Error correction

No.1 2.3.15 CC-Link (Intelligent Device Station)

Description for the CCM_MDIN0-3 signals modified.

<table>
<tr><th colspan="2">V4.00</th><th colspan="2">V4.01</th></tr>
<tr><th>Page</th><th>Description</th><th>Page</th><th>Description</th></tr>
<tr><td>30</td><td>[2.3.15 CC-Link Pins (Intelligent Device Station)]
<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Shared Port</th><th>Active</th><th>Level during Reset</th></tr>
<tr><td>CCM_LINKERRZ</td><td>Output</td><td>Link error LED control output</td><td>P20</td><td>Low</td><td rowspan="5">Note</td></tr>
<tr><td>CCM_ERRZ</td><td>Output</td><td>Error LED control output</td><td>P21</td><td>Low</td></tr>
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<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>Input</td><td>Mode setting switch input</td><td>P62-P65</td><td>—</td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>Input</td><td>Station no. setting switch input</td><td>P70-P77</td><td>—</td></tr>
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<tr><td>CCM_MDIN0-
CCM_MDIN3</td><td>Input</td><td>Transfer rate and mode setting switch input</td><td>P62-P65</td><td>—</td></tr>
<tr><td>CCM_SNIN0-
CCM_SNIN7</td><td>Input</td><td>Station no. setting switch input</td><td>P70-P77</td><td>—</td></tr>
</table></td></tr>
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No.2 3.14.1(1) External MCU Interface

Descriptions for interface system, synchronous relationship, and buffer function modified.

V4.00		V4.01	
Page	Description	Page	Description
58	**[3.14.1(1) External MCU Interface]** - Interface system ➢ SRAM (Read, Write) with WAIT output ➢ Page ROM (Read) with WAIT output - Synchronization-related ➢ HBUSCLK sync, Async (set by HIFSYNC pin) **Caution. When you use asynchronous mode, please input Low into a HBUSCLK pin.** - Bus width ➢ 32-bit, 16-bit (set by BUS32EN pin) **Remark. 8 bit bus width is not supported.** - Transfer data size ➢ 32-bit, 16-bit, 8-bit - Buffer function ➢ Write buffer: 1 step ➢ Read buffer: Max. 32-Byte prefetch supported - Transfer type ➢ Single transfer ➢ Page read transfer - Timing control function	58	**[3.14.1(1) External MCU Interface]** - Interface system ➢ Asynchronous SRAM with wait control (for reading and writing) ➢ Page ROM reading with wait control - Synchronous relationship (set up with the HIFSYNC pin) ➢ HBUSCLK synchronous mode (max. 50 MHz), asynchronous mode **Caution: Drive the HBUSCLK pin to low when asynchronous mode is to be used.** - Bus width (set up with the BUS32EN pin) ➢ 32 bits / 16 bits **Remark: The module does not support 8-bit bus width.** - Transfer data size ➢ 32 bits / 16 bits / 8 bits - Buffer function ➢ Write buffer: Two stages (synchronous mode is selected) or one stage (asynchronous mode is selected) ➢ Read buffer: Advance reading of up to 32 bytes is possible. - Transfer type ➢ Single transfer ➢ Page read transfer - Timing control function

No.3 3.14.1(2) AHB master port function
Description for address conversion modified.

V4.00		V4.01	
Page	Description	Page	Description
58	**[3.14.1(2) AHB master port function]** - AMBA Ver2.0 following ➢ 32-bit AHB-Lite ➢ Little endian fixed - Address conversion ➢ Accusable to 2Mbyte area in AHB memory area (4GByte) from external MPU - Bus sizing function ➢ External 16-bit → 32-bit - Error response function ➢ Output interrupt request (HERROUTZ) in case of receiving error response ➢ Stored the access information of the cause of error in the register	59	**[3.14.1(2) AHB master port function** - AMBA Ver. 2.0 compliant ➢ 32-bit AHB-Lite ➢ Little endinan fixed - Address conversion ➢ 4-Gbyte resource in the AHB memory area can be assigned as the area for the external MCU interface. - Bus sizing ➢ External 16-bit → 32-bit - Error response ➢ Outputs an interrupt request HERROUTZ in response to reception of an error ➢ Access information which involves the error source is stored in the register

No.4 3.14.1(3) Status check function
Applicable modes explicitly noted.

V4.00		V4.01	
Page	Description	Page	Description
59	**[3.14.1(3) Status check function]** - Check status of: ➢ Internal reset ➢ HIFSYNC pin and BUS32EN pin states	59	**[3.14.1(3) Status check function]** - Check status of: ➢ Internal reset (available in synchronous/asynchronous SRAM interface mode) ➢ The HIFSYNC pin, the BUS32EN pin

No.5 3.15.1 Features

Expression alignment from "state" to "wait"

V4.00		V4.01	
Page	Description	Page	Description
60	**[3.15.1 Features]** - Memory controller supporting Page ROM, ROM, SRAM - 32- or 16-bit data Bus - Static memory control function ➢ Supports SRAM and peripheral devices with SRAM interface ➢ Page ROM support (supported CSZ0 only) ➢ Four chip select signals are available (CSZ0-CSZ3) CSZ0 : Page ROM / SRAM : 1000 0000H-13FF_FFFFH (64MByte) CSZ1 : SRAM only : 1400 0000H-17FF_FFFFH (64MByte) CSZ2 : SRAM only : 1800 0000H-1BFF_FFFFH (64MByte) CSZ3 : SRAM only : 1C00 0000H-1FFF_FFFFH (64MByte) - Programmable wait function ➢ Address setting wait ➢ Data wait ➢ Write recovery wait ➢ Idle state	60	**[3.15.1 Features]** - Memory controller supporting Page ROM, ROM, SRAM - 32- or 16-bit data Bus - Static memory control ➢ SRAM and I/O connection ➢ Page ROM connection (CSZ0 only) ➢ Four chip select signals are available (CSZ0-CSZ3) CSZ0: Page ROM / SRAM: 1000 0000H-13FF_FFFFH (64 Mbytes) CSZ1: SRAM only: 1400 0000H-17FF_FFFFH (64 Mbytes) CSZ2: SRAM only: 1800 0000H-1BFF_FFFFH (64 Mbytes) CSZ3: SRAM only: 1C00 0000H-1FFF_FFFFH (64 Mbytes) - Programmable wait ➢ Address setup wait ➢ Data wait ➢ Write recovery wait ➢ Idle wait

No.6 3.16.1 Features

Pin names for wait signal modified.

V4.00		V4.01	
Page	Description	Page	Description
61	**[3.16.1 Features]** **Remark. Each CS can be set between 1000_0000H - 1FFF_FFFFH by the programmable SMADSEL register.** - Programmable wait setting functions ➢ Data wait ➢ Write recovery wait ➢ Idle state - Memory access frequency option (by dividing 100MHz signal by 2 to 6) - Up to four wait state signals available (WAITZ0 - WAITZ3)	61	**[3.16.1 Features]** **Remark. Chip select areas can be assigned to the area between addresses 1000_0000H - 1FFF_FFFFH by using the SMADSEL register (specified in 16-MB units).** - Programmable wait - Memory access frequency (by dividing 100 MHz signal by 2 to 6) - Up to four wait state signals available (WAITZ, WAITZ1 to WAITZ3)

No.7 3.17.1 Features

ECC error interrupt functions added.

V4.00		V4.01	
Page	Description	Page	Description
62	**[3.17.1 Features]** - 128-bit (32-bit x 4) read buffer - Low latency : ➢ Read latency: 2 (1 for accessing read buffer) ➢ Write latency: 1 - 32-bit AHB Bus - 128-bit RAM data bus width (without ECC circuit) - Selectable 16- or 32-bit transfer size - Burst transmission: single, imprecise burst, precise burst (INCR4/8/16, WRAP4/8/16) - Little endian fixed	62	**[3.17.1 Features]** - 128-bit (32-bit × 4) read buffer - Latency: latency is 2 in read access in general but 1 in the case of hitting the read buffer. latency is 1 in write access. - AHB bus width: 32 bits - RAM data bus width: 128 bits (without ECC circuit) - Transfer size: 16- or 32-bit transfer selectable - Burst transfer: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16) - Little endian fixed - ECC response: 1-bit error correction, 2-bit error detection

No.8 3.17.2 Read Buffer

Operation of the AHB bus at occurrence of a 2-bit ECC error modified.

V4.00		V4.01	
Page	Description	Page	Description
62	**[3.17.2 Read buffer features]** - 128-bit (32bit x 4) read buffer - Reply to AHB with 0 wait in cases of accessing read buffer - Clear the data in the read buffer in case of 2-bit ECC error - A 2-bit ECC error at the time of the read response generates an ECC error interrupt and treats it as an error response of the AHB bus.	62	**[3.17.2 Read Buffer]** - 128-bit (32bit × 4) read buffer - Response to the AHB involves no waiting in the case of hitting the read buffer - Clear the data in the read buffer when a 2-bit ECC error occurs. - A 2-bit ECC error at the time of the read response generates an ECC error interrupt.

No.9 3.18 Data RAM

Expression of Header Endec modified.

V4.00		V4.01	
Page	Description	Page	Description
63	**[3.18 Data RAM]** Data RAM is 512Kbytes of memory that can be accessed from AHB and the Ethernet Accelerator (Header Endec (encoder/decoder)).	63	**[3.18 Data RAM]** The internal data RAM is a 512-Kbyte RAM that can be accessed from the AHB and Header Endec (communication bus).

No.10 3.18.1 Features

ECC error interrupt functions are added.

V4.00		V4.01	
Page	Description	Page	Description
63	**[3.18.1 Features]** - AHB latency: ➢ Read / write latency 1 (latency 2 for read access after write access) - Communication bus latency : 1 for read /write access - Round-robin bus arbitration - 32-bit AHB bus width - 128-bit Communication bus width - 128-bit RAM Bus width (without ECC) - AHB transfer size : 8/16/ 32-bit selectable - Communication bus transfer size : 8/16/32/128-bit selectable - Burst transmission : single, imprecise burst, precise burst (INCR4/8/16, WRAP4/8/16) - Little endian fixed	63	**[3.18.1 Features]** - AHB latency: latency is 1 in read and write access (latency is 2 in read access following write access). - Communication bus latency: latency is 1 in read and write access - Arbitration of access when contention arises: Round robin - AHB bus width: 32 bits - Communication bus width: 128 bits - RAM bus width: 128 bits (without ECC circuit) - AHB transfer size: 8/16/ 32-bit selectable - Communication bus transfer size: 8/16/32/128-bit selectable - Burst transmission: single burst transfer, burst transfer of the required length, burst transfer of the fixed length (INCR4/8/16, WRAP4/8/16) - Little endian fixed - ECC response: 1-bit error correction, 2-bit error detection

No.11 3.19.1 Features

ECC error interrupt functions are added.

V4.00		V4.01	
Page	Description	Page	Description
64	**[3.19.1 Features]** - Communication bus latency: 1 for read / write access - Fixed-priority communication bus arbitration - 128-bit communication bus width - 128-bit RAM bus width (without ECC) - Communication bus transfer size: 8/16/32/128-bit selectable	64	**[3.19.1 Features]** - Communication-bus latency: latency is 1 in read and write access - Arbitration of access when contention arises: Fixed priority (the communication bus is given priority) - Communication bus width: 128 bits - RAM bus width: 128 bits (without ECC circuit) - Communication-bus transfer size: 8-, 16-, 32-, 128-bit transfer selectable - ECC response: 1-bit error correction, 2-bit error detection

No.12 3.20.1 Features

Supported functions; Internal DMA, Buffer Allocator, and Header EnDec are added.

V4.00		V4.01	
Page	Description	Page	Description

65	**[3.20.1 Features]**
	
	- Task Scheduler
	  ➢ Hardware ISR : Maximum 32 selectable from 128 interrupts
	  ➢ Contexts : 64
	  ➢ Semaphores : 128
	  ➢ Events : 64
	  ➢ Mailboxes : 64
	  ➢ Mailbox elements : 192
	  ➢ Context priorities: 16
	- Hardware Function Manager
		65	**[3.20.1 Features]**
			
			- Task Scheduler
			  ➢ Hardware ISR: 32 routines selectable from 128 interrupt sources
			  ➢ Number of contexts elements: 64
			  ➢ Number of semaphore identifiers: 128
			  ➢ Number of event identifiers: 64
			  ➢ Number of mailbox identifiers: 64
			  ➢ Number of mailbox elements: 192
			  ➢ Number of context priority levels: 16
			- Hardware Function Manager
			- Internal DMA
			- Buffer allocator
			- Header EnDec

No.13 4.4 DC Characteristics

Statements for 5kΩ resistor was deleted from the parameter "Input leakage current" of Table 4.6.

V4.00

Page	Description
71	**[4.4 DC Characteristics]** [Table 4.6 DC Characteristics (V_{DD} = 3.3±0.3V, T_A = -40 to +85ºC) (1/2)]

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current (3.3 V buffer)	I_I	V_I = V_{DD} or GND	Normal input	—	—	±10	µA
		V_I = GND	With Pull-up resistor (5 kΩ)	−293.8	−645.7	−1181.3	µA
			With Pull-up resistor (50 kΩ)	−28.9	−65.7	−129.8	µA
		V_I = V_{DD}	With Pull-down resistor (50 kΩ)	10.2	43.4	83.9	µA
Input leakage current (5V- Tolerant buffer)	I_I	V_I = GND	With Pull-up resistor (50 kΩ)	39.0	—	100.9	µA

V4.01

Page	Description
71	**[4.4 DC Characteristics]** [Table 4.6 DC Characteristics (V_{DD} = 3.3±0.3V, T_A = -40 to +85ºC) (1/2)]

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current (3.3V buffer)	I_I	V_I = V_{DD} or GND	Normal input	—	—	±10	µA
		V_I = GND	With pull-up resistor (50 kΩ)	−28.9	−65.7	−129.8	µA
		V_I = V_{DD}	With pull-down resistor (50 kΩ)	10.2	43.4	83.9	µA
Input leakage current (5V-tolerant buffer)	I_I	V_I = GND	With pull-up resistor (50 kΩ)	39.0	—	100.9	µA

No.14 4.4 DC Characteristics

The symbol for the "Output voltage, high" of Table 4.7 was changed from "IOL" to "IOH".

V4.00

Page	Description
71	**[4.4 DC Characteristics]** [Table 4.7 DC Characteristics (V_{DD} = 3.3±0.3V, T_A = -40 to +85ºC) (2/2)]

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL}	I_{OL} = 0mA	3.3V buffer	—	—	0.1	V
			5V-Tolerant buffer	—	—	0.1	V
Output voltage, high	V_{OH}	I_{OL} = 0mA	3.3V buffer	V_{DD}−0.1	—	—	V
			5V-Tolerant buffer	V_{DD}−0.1	—	—	V

V4.01

Page	Description
71	**[4.4 DC Characteristics]** [Table 4.7 DC Characteristics (V_{DD} = 3.3±0.3V, T_A = -40 to +85ºC) (2/2)]

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL}	I_{OL} = 0mA	3.3V buffer	—	—	0.1	V
			5V-Tolerant buffer	—	—	0.1	V
Output voltage, high	V_{OH}	I_{OH} = 0mA	3.3V buffer	V_{DD}−0.1	—	—	V
			5V-Tolerant buffer	V_{DD}−0.1	—	—	V