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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan **Renesas Electronics Corporation**

Product Category	MPU/MCU	IPU/MCU		TN-RL*-A0136B/E	Rev.	2.00
Title	Notification of Corrections to Errors Amendments to Descriptions and Limitations Capacitive Sensing Unit	on the	Information Category	Technical Notification		
		Lot No.		RL78/G22 User's Man	ual: Hard	ware
Applicable Product	RL78/G22 Group and RL78/G23 Group	All lots	Reference Document	R01UH0978EJ0100 (I RL78/G23 User's Man Rev. 1.30 R01UH0896EJ0130 (J	Dec. 2022 ual: Hard lan. 2024	2) ware)

1. Corrections to Errors

The following errors in Revision 1.00 of the RL78/G22 User's Manual: Hardware (R01UH0978EJ0100) and Revision 1.30 of the

RL78/G23 User's Manual: Hardware (R01UH0896EJ0130) are to be corrected.

rrections			
	Applicat	ole Page	
Applicable Item	R01UH0978 EJ0100	R01UH0896 EJ0130	Contents
	(RL78/G22)	(RL78/G23)	
Sensor Drive Pulse Output Clock Configuration	Page 1005	Page 1255	Incorrect descriptions
CTSU control registers AL and AH (CTSUCRAL,	Page 1008 to	Page 1259 to	Incorroct descriptions
CTSUCRAH)	Page 1010	Page 1261	
CTSU status register L (CTSUSRL)	Page 1026	Page 1276	Incorrect descriptions
CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)	Page 1027	Page 1277	Incorrect descriptions
CTSU sensor unit clock control registers AL, AH, BL, and BH (CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, CTSUSUCLK3)	Page 1033, Page 1034	Page 1283, Page 1284	Incorrect descriptions
CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)	Page 1035	Page 1285	Incorrect descriptions

Corre

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

2. Effects of the Errors on Applicable Products

In descriptions of the capacitive sensing unit in the user's manuals for the applicable products stated above, SUCLK frequencies that are outside the range at which SUCLK is capable of operating are included. Setting an SUCLK frequency that is outside this range according to the erroneous descriptions may lead to an incorrect result of touch measurement.

However, if the QE (Quick and Effective Tool Solution) for Capacitive Touch tool V3.3.0, a development assistance tool for capacitive touch sensors, is in use and multi-frequency measurement is selected (the default setting), majority decision will proceed. Accordingly, the final result of touch measurement is considered unlikely to be incorrect in such cases. See 2.1, Effects on Touch Detection for details.

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Corrections in the User's Manual: Hardware

			Corrections and Applicable It	ems		Deges in this
No.		Document No.	English	R01UH0978 EJ0100 (RL78/G22)	R01UH0896 EJ0130 (RL78/G23)	document for corrections
1.1	Sensor	Drive Pulse Output C	lock Configuration	Page 1005	Page 1255	Page 3
1.2	CTSU C	control registers AL ar RAH)	nd AH (CTSUCRAL,	Page 1008 to Page 1010	Page 1259 to Page 1261	Page 4 to Page 6
1.3	.3 CTSU status register L (CTSUSRL)			Page 1026	Page 1276	Page 7
1.4	I.4 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)			Page 1027	Page 1277	Page 8
1.5	CTSU sensor unit clock control registers AL, AH, BL, and BH (CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, CTSUSUCLK3)			Page 1033, Page 1034	Page 1283, Page 1284	Page 9, Page 10
1.6	CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)			Page 1035	Page 1285	Page 11

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G22 and RL78/G23 Correction for incorrect description notice

Document Number	Issue Date	Rev.	Description
TN-RL*-A0136A/E	May 28, 2024	1.00	First edition issued
TN-RL*-A0136B/E	Jun. 19, 2024	2.00	Regarding page 6, the register symbols were corrected.
			Regarding page 9, "SUCLK Multiplication Rate Setting" was corrected
			to "STCLK Multiplication Rate Setting".



1.1 Sensor Drive Pulse Output Clock Configuration

Incorrect:

Page 1005 (RL78/G22), Page 1255 (RL78/G23)



(omitted)

Date: Jun. 19, 2024

Correct:





1.2 CTSU control registers AL and AH (CTSUCRAL, CTSUCRAH)

Incorrect:

Page 1008 (RL78/G22), Page 1259 (RL78/G23)

				(omitted)				
Address: After reset: R/W:	F0500H, F050 0000H R/W	01H (CTSUCF	RAL), F0502H	I, F0503H (C1	SUCRAH)			
Symbol	15	14	13	12	11	10	9	8
CTSUCRAH	DCBACK	DCMODE			STCL	K[5:0]		
	7	6	5	4	3	2	1	0
	ECMODE	SDPSEL	POSE	:L[1:0]	LOAD1	LOAD0	ATUNE2	0

Date: Jun. 19, 2024

Correct:

Address:	F0500H, F0501H (CTSUCRAL), F0502H, F0503H (CTSUCRAH)
After reset:	0000H
R/W:	R/W

Symbol	15	14	13	12	11	10	9	8
CTSUCRAH	DCBACK	DCMODE			STCL	K[5:0]		
-								
	7	6	5	4	3	2	1	0
	PCSEL	SDPSEL	POSE	L[1:0]	LOAD1	LOAD0	ATUNE2	0

Date: Jun. 19, 2024

Page 1009 (RL78/G22), Page 1260 (RL78/G23)

-				(omitted)				
FCM	ODE			Sensor unit clock (SUCLK) Select				
Ç)	SUCLK	SUCLK is used as frequency diffusion clock.					
1	ļ	SUCLK	is used as recov	ery clock for multi-clock measurement.				
		To use S	SUCLK as recove	ery clock, set the CTSUDBGR1.CCOCLK bit to 1.				
• Whe	n the EO	MODE b	it is 0 (SUCLK u	sed as frequency diffusion clock)				
As sp CTSI	Decified	Lin the C	TSUTRIM1.SUAD 2·01	0.JD[7:0], CTSUCRBH.SSCNT[1:0], and				
SUCI	K is ge	enerated	when the digital	oscillator oscillates and the frequency is spectrum-diffused.				
• When As.s. is.ge Befo CTSI The.r meas CTSI When CTSI	n the EG pecifiec nerated re settil JSUCLI SUCLI SUCLI n the EG JSUCLI	CMODE is Lin the C Lwhen th ng the EC K3 regist y is perfo nt. The S K3 regist CMODE b K3 regist	s 1 (SUCLK used TSUSUCLK0, CT te clock recovery MODE bit to 1, s er. ormed in status 1 UADJx bits in the er are updated b bit is 1, do not ch er setting.	Las recovery clock for multi-clock measurement) SUSUCLK1, CTSUSUCLK2, or CTSUSUCLK3 register, SUCLK y control is performed. Set the CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or 0. (non-measurement state) for all selected clocks during. e CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or y recovery. (x = 0. to.3). ange the CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, or				
≲Relat	ionship	betweer	SDPSEL and FO					
	SD	PSEL	FCMODE	Operation				

		sepesationsess
0	Q	Random pulse mode (CTSU compatible setting)
1	1	Sensor unit clock (SUCLK) mode Used for multi- clock measurement
Other than above		Setting prohibited

	(omitted)
PCSEL	Voltage Booster Clock Select
0	Sensor drive pulse
1	STCLK
This bit selects	s the clock for the voltage boost circuit.

Page 1010 (RL78/G22), Page 1261 (RL78/G23)

SDPSEL	Sensor Drive Pulse Select
0	Random pulse mode (CTSU compatible setting)
	The operating clock divided by the settings of the CTSUSO1.SDPA[7:0] bits is
	used as the base clock, and the sensor drive pulse is obtained by phase-
	shifting the base clock using the random number generated according to the
	settings of the CTSUCRBL.PRMODE[1:0] and CTSUCRBL.PRRATIO[3:0] bits. It.
	is also possible to apply jitter by the frequency diffusion clock.
1	Sensor unit clock (SUCLK) mode
	The sensor drive pulse is obtained by applying frequency recovery based on
	fCLK to generate SUCLK and dividing it by the settings of the
	CTSUSO1.SDPA[7:0] bits.
The SDPSEL	bit selects the sensor drive pulse.

(omitted)

SDPSEL	Sensor Drive Pulse and SUCLK Select
0	Random pulse mode
	Sensor drive pulse
	fclk divided by the settings of the CTSUCRAL.CLK[1:0] and CTSUSO1.SDPA[7:0] bits are
	used as the base clock, and the sensor drive pulse is obtained by phase-shifting the base
	clock using the random number generated according to the settings of the
	CTSUCRBL.PRMODE[1:0] and CTSUCRBL.PRRATIO[3:0] bits. It is also possible to apply
	jitter by the frequency diffusion clock.
	• SUCLK
	The built-in oscillator is operated with the settings of CTSUCRBH.SSCNT[1:0],
	CTSUCRBH.SSMOD[2:0], and CTSUTRIM1.SUADJD[7:0] to generate SUCLK with frequen
	spread spectrum.
1	Hi-resolution pulse mode
	Sensor drive pulse
	The clock (base clock) obtained by dividing SUCLK by the CTSUSO1.SDPA[7:0] bits is
	used as the sensor drive pulse.
	• SUCLK
	By setting the CTSUSUCLKX register (x = 0 to 3), clock recovery control is performed and
	SUCLK is generated.
	Recovery updates the CTSUSUCLKx.SUADJx[7:0] bits.
	Set the CTSUSUCLKx register before setting this bit to 1.
	Do not change the CTSUSUCLKx register while this bit is 1.
	hit toggles between random pulse made and hi resolution pulse made. This selection
ne SDPSEL	bit toggles between random pulse mode and ni-resolution pulse mode. This selection
hanges how	the sensor drive pulse and SUCLK are generated.



1.3 CTSU status register L (CTSUSRL)

Incorrect:

Page 1026 (RL78/G22), Page 1276 (RL78/G23)

		(omitted)
MFC[1:0]		Multi-clock Counter
0	0	Multi-clock 0
0	1	Multi-clock 1
1	0	Multi-clock 2
1	1	Multi-clock 3
The MFC[1:0]	bits indicate the	ne clock that is being measured during multi-clock measurement
(CTSUCRAH	FCMODE = 1)	L

Date: Jun. 19, 2024

Correct:

		(omitted)
MFC	C[1:0]	Multi-clock Counter
0	0	Multi-clock 0
0	1	Multi-clock 1
1	0	Multi-clock 2
1	1	Multi-clock 3
The MFC[1:0] bits indicate t	he clock that is being measured during multi-clock measurement
(CTSUCRAH	.SDPSEL = 1).	



1.4 CTSU sensor offset registers 0 and 1 (CTSUSO0, CTSUSO1)

Incorrect:

Page 1027 (RL78/G22), Page 1277 (RL78/G23)

						(omitte	d)		
		S	DPA[7:0]				Senso	r. Driving	Pulse Divisor Setting
•)	When CT	SUCRAH	.SDPSEL	.=.0					
-	The opera	ting clock	is divide	d to gene	rate a bas	se clock to	be the s	ource of s	sensor drive pulse. These
		so avaliai		ung the v	ollage sta	abilization		IE 0100.	
	0	0	0	0	0	0	0	0 O	perating clock divided by 2 ^{Note}
	0	0	0	0	0	0	0	1 0	perating clock divided by 4
	0	0	0	0	0	0	1	0 O	perating clock divided by 6
	0	0	0	0	0	0	1	1 0	perating clock divided by 8
	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0 O	perating clock divided by 510
	1	1	1	1	1	1	1	1 0	perating clock divided by 512
	Note	Whe	n jitter ap	plication i	s disable	d (CTSUC	CRBL.SO	FF bit = 1) in the mutual capacitance
		meth	nod, settin	g of SDP	A[7:0] = 0	0000000	B is proh	bited.	
•)	When CT	SUCRAH	SDPSEL	.=1					
٦	The SUCL	K clock is	s divided f	o genera	te a sense	or drive p	ulse.		
				1	1		1		· · · · · · · · · · · · · · · · · · ·
	0	0	0	0	0	0	0	0	SUCLK divided by 1
	0	0	0	0	0	0	0	1	SUCLK divided by 2
	0	0	0	0	0	0	1	0	SUCLK divided by 3
	0	0	0	0	0	0	1	1	SUCLK divided by 4
	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0	SUCLK divided by 255
	1	1	1	1	1	1	1	1	SUCLK divided by 256

Correct:

	SI	DPA[7:0]			Bas	e Clock (Sensor D	Drive Pul	se Frequency Divisor) Setting
Fo	or the ra	ndom pul	se mode	, that is, v	when CT		.SDPSE	EL = 0.	a of sonsor drive pulse. These
bii C ⁻ 2(ts are al TSUSO ² (n+1).	so availa 1.SDPA[7	ble for se 2:0] bits is	tting the	voltage s ase clock	tabilizatio is obtair	on time o ed by fr	of the C	rSU. If the setting of the y-dividing the operating clock by
	0	0	0	0	0	0	0	0	Operating clock divided by 2 ^{Note}
	0	0	0	0	0	0	0	1	Operating clock divided by 4
	0	0	0	0	0	0	1	0	Operating clock divided by 6
	0	0	0	0	0	0	1	1	Operating clock divided by 8
	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0	Operating clock divided by 510
Г	1	1	1	1	1	1	1	1	Operating clock divided by 512
l Fo	Note	Whe meth	en jitter ap nod, setti n pulse n	oplication ng of SDI node, tha	is disabl PA[7:0] = t is, wher	ed (CTSU 0000000 n CTSUC	JCRBL.S 00B is pr RAH.SE	SOFF bi ohibited	t = 1) in the mutual capacitance I.
Fo Th Th	Note or the hi- he SUCL SUCLK	Whe meth resolutio .K clock i .K freque = STCLK	en jitter ap nod, setti n pulse n s divided ncy can t ×SUCLK	oplication ng of SD node, tha to gener be calcula multiplica	is disabl PA[7:0] = t is, when ate a sen ated from ation rate	ed (CTSU 0000000 n CTSUC sor drive the follow setting m	JCRBL. 00B is pr RAH.SE pulse. wing exp ade by th	SOFF bi rohibited DPSEL = pression ne CTSL	t = 1) in the mutual capacitance I. = 1. JSUCLKx.SUMULTIx[7:0] bits
Fa Th Th	Note or the hi- he SUCL SUCLK SUCLK the settin JCLK clo	Whe meth K clock i: K freque = STCLK ng of the C ock by 2(n	n jitter ap nod, settii s divided ncy can t ×SUCLK CTSUSO ⁴ +1).	oplication ng of SD node, tha to gener- be calcula multiplica .SDPA[7	is disabl PA[7:0] = t is, when ate a sen ated from ation rate :0] bits is	ed (CTSU 0000000 n CTSUC sor drive the follor setting m n, the ser	JCRBL.S DOB is pr RAH.SE pulse. wing exp ade by th asor drive	SOFF bi rohibited DPSEL = pression ne CTSL e pulses	t = 1) in the mutual capacitance = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the
	Note or the hi- he SUCL ne SUCL SUCLK the settin JCLK clo	Whe meth K clock i: K freque = STCLK ng of the C ock by 2(n	en jitter ap nod, setti n pulse n s divided ncy can t ×SUCLK CTSUSO1 +1).	pplication ng of SD node, tha to gener be calcula multiplica SDPA[7	is disabl PA[7:0] = t is, when ate a sen ated from ation rate :0] bits is	ed (CTSU 0000000 n CTSUC sor drive the follor setting m n, the ser	JCRBL.S 00B is pr RAH.SE pulse. wing exp ade by th asor drive	SOFF bi ohibited DPSEL = pression ne CTSL e pulses	t = 1) in the mutual capacitance t. = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the 0 SUCLK divided by 2
	Note or the hi- ne SUCL ne SUCL SUCLK SUCLK the settin JCLK clo	Whe meth resolutio .K clock i .K freque = STCLK ig of the C ock by 2(n	en jitter ap nod, setti n pulse n s divided ncy can b ×SUCLK CTSUSO ⁴ +1).	pplication ng of SD node, tha to gener be calcula multiplica .SDPA[7 0 0	is disabl PA[7:0] = t is, when ate a sen ated from ated from ation rate :0] bits is 0 0	ed (CTSU 0000000 n CTSUC sor drive the follor setting m n, the ser 0 0	JCRBL.S 00B is pr RAH.SE pulse. wing exp ade by th asor drive 0 0	SOFF bi ohibited DPSEL = pression ne CTSU = pulses	t = 1) in the mutual capacitance 1. = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the 0 SUCLK divided by 2 1 SUCLK divided by 4
	Note For the hi- he SUCL SUCLK SUCLK clo 0 0 0 0	Whe meth resolutio .K clock i .K freque = STCLK ng of the C ock by 2(n 0 0	n jitter ap nod, settii n pulse n s divided ncy can b ×SUCLK CTSUSO1 +1).	pplication ng of SD node, tha to gener- be calcula multiplica .SDPA[7 0 0 0	is disabl PA[7:0] = t is, when ate a sen ated from ation rate :0] bits is 0 0 0	ed (CTSU 0000000 or CTSUC sor drive the follor setting m n, the ser 0 0 0	UCRBL.5 00B is pr RAH.SE pulse. wing exp ade by th nsor drive 0 0	SOFF bi ohibited DPSEL = Dression ne CTSL e pulses	t = 1) in the mutual capacitance t = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the 0 SUCLK divided by 2 1 SUCLK divided by 4 0 SUCLK divided by 6
	Note For the hi- he SUCL SUCLK the settin JCLK clo 0 0 0 0 0	Whe meth K clock i K freque = STCLK g of the C ock by 2(n 0 0 0	n jitter ap nod, settii n pulse n s divided ncy can t ×SUCLK CTSUSO ++1). 0 0 0	pplication ng of SD node, tha to gener- be calcula .SDPA[7 0 0 0 0	is disabl PA[7:0] = t is, when ate a sen ated from ation rate :0] bits is 0 0 0 0	ed (CTSU 0000000 sor drive the follow setting m n, the ser 0 0 0	JCRBL.S DOB is pr RAH.SE pulse. wing exp ade by th nsor drive 0 0 0 1	SOFF bi rohibited DPSEL = Dression ne CTSL = pulses	t = 1) in the mutual capacitance t = 1) in the mutual capacitance t = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the 0 SUCLK divided by 2 1 SUCLK divided by 4 0 SUCLK divided by 6 1 SUCLK divided by 8
	Note or the hi- he SUCL SUCLK SUCLK clo 0 0 0 0 0 0 0 0 0 0 0 0 0	Whe meth resolutio .K clock i .K freque = STCLK g of the C ock by 2(n 0 0 0 0 0 0	en jitter ap nod, setti n pulse n s divided ncy can b ×SUCLK CTSUSO1 +1).	pplication ng of SD node, tha to gener- be calcula .SDPA[7 0 0 0 0	is disabl PA[7:0] = t is, when ate a sen ated from ation rate :0] bits is 0 0 0 0 0	ed (CTSU 0000000 or CTSUC sor drive the follor setting m n, the ser 0 0 0 0	JCRBL.5 00B is pr RAH.SE pulse. wing exp ade by th sor drive 0 0 1 1 1	SOFF bi rohibitec DPSEL = Dression ne CTSL = pulses	t = 1) in the mutual capacitance t = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the 0 SUCLK divided by 2 1 SUCLK divided by 4 0 SUCLK divided by 6 1 SUCLK divided by 8 : :
	Note For the hi- he SUCL SUCLK SUCLK the settin JCLK clo 0 0 0 0 0 1	Whe meth resolutio .K clock i: .K freque = STCLK ig of the C ock by 2(n 0 0 0 0 0 0 1	n jitter ap nod, setti n pulse n s divided ncy can t ×SUCLK CTSUSO ¹ +1). 0 0 0 0 0 0	pplication ng of SD node, tha to gener be calcula multiplica .SDPA[7 0 0 0 0 0 0 0 1	is disabl PA[7:0] = t is, when ated from ated from ation rate :0] bits is 0 0 0 0 0 1	ed (CTSU 0000000 a CTSUC sor drive the follor setting m n, the ser 0 0 0 0 0 1	JCRBL.S DOB is pr RAH.SE pulse. wing exp ade by th asor drive 0 0 1 1 1 1	SOFF bi rohibited DPSEL = Dression ne CTSL = pulses	t = 1) in the mutual capacitance t = 1) in the mutual capacitance a. = 1. JSUCLKx.SUMULTIx[7:0] bits are obtained by frequency-dividing the 0 SUCLK divided by 2 1 SUCLK divided by 2 1 SUCLK divided by 6 1 SUCLK divided by 8 : : 0 SUCLK divided by 5 10 SUCLK divid



1.5 <u>CTSU sensor unit clock control registers AL, AH, BL, and BH</u> (CTSUSUCLK0, CTSUSUCLK1, CTSUSUCLK2, CTSUSUCLK3)

Incorrect:

Page 1033 (RL78/G22), Page 1283 (RL78/G23)

SUMUL	Tlx[7:0]			SL	ICLK M	ultiplicat	tion Rat	e Setting
The SUM	ULTIx[7	:0] bits	set the	multipli	ication	rate of S	STCLK	assuming 0.5 MHz (divided)
іськ)) to (jenerate	SUCLI	ς.					
STCLK is	compa	red with	1 SUCLI	K divide	ed by th	is settir	ıg. Bas	ed on the comparison result.
he SUAI)Jx[7:0]	bits are	e update	ed. The	target of	clock fr	eauenc	v is 32 to 80 MHz.
******						******		,
		r	r	r	r	1		
0	0	0	0	0	0	0	0	× 1
:	:	:	:	:	:	:	:	:
: 0	: 0	: 1	: 1	: 1	: 1	: 1	: 1	: × 64
: 0 :	: 0 :	: 1 :	: 1 :	: 1 :	: 1 :	: 1 :	: 1 :	: × 64 :
: 0 : 0	: 0 : 1	: 1 : 1	: 1 : 1	: 1 : 1	: 1 : 1	: 1 : 1	: 1 : 1	: × 64 : × 128
: 0 : 0 :	: 0 : 1 :	: 1 : 1	: 1 : 1 :	: 1 : 1 :	: 1 : 1 :	: 1 : 1 :	: 1 : 1 :	: × 64 : × 128 :

Date: Jun. 19, 2024

Correct:

_						(omit	tted)		
5	SUMULT	Flx[7:0]			ST	FCLK Mu	ultiplicat	ion Rate	e Setting
Th tak	e SUML ken to be	JLTIx[7: e at 0.5	0] bits s MHz, ol	et the fr otained	equenc by frequ	y multipl iency-div	lier for g viding f _c	eneratir _{:LK}).	ng SUCLK from STCLK (which is
Th	e SUCL	K clock	is capa	ble of op	perating	at a fre	quency	in the ra	ange from 16 MHz to 32 MHz.
lf t	he SUC	LK clocl	k is to b	e used,	ensure	that its f	requenc	cy is witl	hin that range.
ln : this	addition s setting	, the SL g.	IADJx[7	:0] bits a	are upda	ated in r	esponse	e to the	SUCLK frequency generated by
Th	e SUCL	K freque	ency ca	n be cal	culated	from the	e followi	ng expr	ession.
S	UCLK =	= STCLK	(×SUC	LK multi	plicatior	n rate se	etting ma	ade by t	he
С	TSUSU	ICLKx.S	UMULT	ˈlx[7:0] k	oits				
	0	0	0	0	0	0	0	0	× 1

0	0	0	0	0	0	0	0	×
:	:	:	:	:	:	:	:	:
0	0	1	1	1	1	1	1	× 64
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	× 128
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	× 256



Page 1034 (RL78/G22), Page 1284 (RL78/G23)

SUADJx[7:0]	SUCLK Frequency Adjustment
The SUADJx[7:0)] bits set the initial value of the SUCLK frequency.
The drift is adju	sted and the SUADJx[7:0] value is updated by the clock recovery function.
The output freq	uency varies from the set value in each MCU. The SUCLK frequency is
adjusted based	on the register set value as an initial value and the register value is updated
by the clock rec	overy control.

Date: Jun. 19, 2024

SUADJx[7:0]

SUCLK Frequency Adjustment

The SUADJx[7:0] bits set the initial value of the SUCLK frequency.

The clock recovery function corrects SUCLK for clock drift, resulting in updating of this register value.

Do not write values to these registers.



1.6 CTSU trimming registers AL and AH (CTSUTRIM0, CTSUTRIM1)

Incorrect:

Page 1035 (RL78/G22), Page 1285 (RL78/G23)

(omitted)

SUADJD[7:0] SUCLK Frequency Adjustment

The SUADJD[7:0] bits hold the initial value for generating approx. 64 MHz, which is set

at the factory. When FCMODE is 0, this set value is input to the digital oscillator.

Do not modify this initial value set at the factory.

(omitted)

Date: Jun. 19, 2024

Correct:

(omitted)	
-----------	--

SUADJD[7:0]	SUCLK Frequency Adjustment
The SUADJD[7:0]	bits are used to adjust the SUCLK frequency in the random pulse mode
(selected by CTSU	CRAH.SDPSEL = 0).
These bits hold the	initial setting at the time of shipment. Do not write values to them.



2.1.1 Problem

The usable range of SUCLK frequency is stated to be 32 MHz to 80 MHz, but the range of frequency at which SUCLK is actually capable of operating is 16 MHz to 32 MHz. Proceeding with touch measurement with the SUCLK frequency set to a value outside the range from 16 MHz to 32 MHz may lead to the result of touch detection in the first cycle of SUCLK being undefined. This is likely to result in an error of \pm 1 being generated in the value of the counter for the results of touch measurement. The effect of this on the results of touch measurement is considered to be negligible.

2.1.2 Workaround for the Problem

The SUCLK frequency is determined by the following expression. Set the CTSUCRAL.CLK[1:0], CTSUCRAH.STCLK[5:0], and CTSUSUCLK0 and CTSUSUCLK1.SUMULTIx[7:0] bits so that the SUCLK frequency is in the range from 16 MHz to 32 MHz.

SUCLK = (f_{CLK} frequency/CLK/STCLK) × SUMULTIx setting

CLK above refers to the CTSUCRAL.CLK[1:0] setting. f_{CLK} is frequency-divided by the value corresponding to this setting in setting the operating clock.

STCLK above refers to the CTSUCRAH.STCLK[5:0] setting. The operating clock is frequency-divided by the value corresponding to this setting in setting the state clock (STCLK).

SUMULTIx above refers to the CTSUSUCLK0 or CTSUSUCLK1.SUMULTIx[7:0] setting. STCLK is multiplied by the value corresponding to this setting in setting SUCLK.



2.1.3 Effects When the QE for Capacitive Touch Tool V3.3.0, a Development Assistance Tool for Capacitive Touch Sensors, Is in Use

Use of the QE for Capacitive Touch tool, a development assistance tool for capacitive touch sensors, allows the setting of the SUCLK frequency to a value outside the permissible frequency range for SUCLK operation.

Figure 2-1 shows the default settings of the QE tool V3.3.0, which select three-frequency measurement.

Using the SIS driver (an RL78 touch driver) for the CTSU module enables multi-frequency measurement. With the default settings, three-frequency measurement proceeds. Specifically, three frequencies, n, (n-x), and (n+x) MHz, are used for measurement and majority decision proceeds.

With the default settings of the QE tool V3.3.0, the SUCLK frequency for measurement 3 is 36.5 MHz, which is outside the permissible frequency range for SUCLK operation, as indicated by the red text in Figure 2-1.

Setting the frequency to 36.5 MHz may lead to an error of ± 1 being generated in the value of the counter for the results of touch measurement.

However, the final result of touch measurement is considered unlikely to be incorrect because majority decision proceeds in multi-frequency measurement. Corrections concerning this problem will be made in the next revision of the QE tool.

In addition, setting a frequency greater than 32 MHz does not create a risk of damage to the microcontroller.

Figure 2-1 Settings of the QE Tool V3.3.0 for Three-Frequency Measurement (the Default Settings)

elect setting values for ea	ach method ertently or witho	d / touch inte	rface. ling, it could lead	to poor tun	ing results.	
Method Capacitance Type Shield config01 Self Capacitance None	l Pin Target Va Auto	lue of Offset Tuning	Measured Curr Auto	rent Range	Non-Mea Auto	sured Channel
Multi-Clock Measuring Mu System 3 Frequencies 64	ultiplier Rate 1	Multiplier Rate 2 55	Multiplier Rate 3 73	Judgemer Default	nt Type	
		The Social Socia	STCLK freque	ncy will b	be 0.5 M	ier setting Hz with the
Example of the default setting	s: s 32 MHz	The S defau	STCLK freque	ncy will b	be 0.5 M	ier setting Hz with the
Example of the default setting When the SUCLK frequency i	s: s 32 MHz Measure	ment 1 Me	STCLK freque It setting.	ncy will b	be 0.5 M	ier setting Hz with the
Example of the default setting When the SUCLK frequency is Frequency multiplier	s: s 32 MHz Measure 64	ment 1 Me	STCLK freque It setting.	Mea	asuremer	ier setting Hz with the
Example of the default setting When the SUCLK frequency is Frequency multiplier SUCLK frequency (MHz)	s: s 32 MHz Measure 64 32.0	ment 1 Me 55 27.	STCLK freque It setting.	Mea Mea 73 36.5	asuremer	ier setting Hz with the
Example of the default setting When the SUCLK frequency is Frequency multiplier SUCLK frequency (MHz) Setting of the CTSUSO1.SDPA[7:0] bits	s: s 32 MHz Measure 64 32.0 3	ment 1 Me 55 27. 3	STCLK freque It setting.	Mea 73 36.5 3	asuremer	ier setting Hz with the
Example of the default setting When the SUCLK frequency is Frequency multiplier SUCLK frequency (MHz) Setting of the CTSUSO1.SDPA[7:0] bits Frequency divisor for the drive pulse	s: s 32 MHz Measure 64 32.0 3 e 8	ment 1 Me 55 27. 3 8	STCLK freque stting. asurement 2	Mea 73 36.5 3 8	asuremer	ier setting Hz with the

