To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

Date: Aug.02.2005

RENESAS TECHNICAL UPDATE

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Renesas Technology Corp.

Product Category	MPU&MCU		Document No.	TN-SH7-A561A/E	Rev.	1.00
Title	Notice for using User Break Controller (UBC)		Information Category	Technical Notification		
Applicable Product	R5S72060W200FPV R5E72060W200FPV	Lot No. ALL	Reference Document	SH7206 Group Hardware Manual (Mar.18.05 REJ09B0191-0100 Rev.1.00)		

There is the notice for using Break on Instruction Fetch Cycle in User Break Controller (UBC).

1. User Break before instruction execution for the instruction following the DIVU or DIVS instruction

Do not set a user break before instruction execution for the instruction following the DIVU or DIVS instruction. If a user break before instruction execution is set for the instruction following the DIVU or DIVS instruction and an exception or interrupt occurs during execution of the DIVU or DIVS instruction, a user break occurs before instruction execution even though execution of the DIVU or DIVS instruction is halted.

2. Setting User Break both before instruction execution and after instuction execution for instruction of the same address

Do not set a user break both before instruction execution and after instruction execution for instruction of the same address. If, for example, a user break before instruction execution on channel 0 and a user break after instruction on channel 1 set at the instruction of the same address, the condition match flag for the channel 1 is set even though a user break on channel 0 occurs before instruction execution.