To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Date: May.31.2005

RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A553A/E	Rev.	1.0
Title	Notice for using Burst ROM interface		Information Category	Technical Notification		
Applicable Product	R5S72060W200FPV R5E72060W200FPV	Lot No. ALL	Reference Document	SH7206 Group Hardware Manual (REJ09B0191-0100 Rev.1.00)		

For Applicable Product, there is a notice in write operation of using Burst ROM interface (clocked asynchronous).

1.Content

There are cases that read/write access for external Bus interface can be invalid just after write access for Burst ROM interface.
In the case of instruction fetch, exception handling for illegal instruction can occur or unexpected instruction can be executed.
In the case of data access, read data can be invalid or write access can be invalid.

2.Conditions

The above invalid access occurs when the following all 3 conditions are satisfied.

(1) Using 16 bit data bus width for Burst ROM interface (clocked asynchronous)
(CSnBCR.TYPE[2:0]=B'001 and CSnBCR.BSZ[1:0]=B'10)

(2) 4 burst length (CSnWCR.BST[1:0]=B'10)

(3) Write-back operation by operand CACHE or 16-byte unit write access by DMAC for Burst ROM interface (clocked asynchronous) which is set as above (1) and (2) conditions.

3. Notice

Notice for the above invalid access is shown below.

In the case of using Burst ROM interface (clocked asynchronous) (CSnBCR.TYPE[2:0]=B'001),
If using 16 bit data bus width (CSnBCR.BSZ[1:0]=B'10) and 4 burst length (CSnWCR.BST[1:0]=B'10),

(1) When there is CPU write access for the Burst ROM interface (clocked asynchronous),
Please use write access for non-cacheable interface or set Operand CACHE as write-through mode.

(2) When there is DMA write access for the Burst ROM interface (clocked asynchronous),
Please use Byte/word/Long-Word unit access or set LSB 4 bits of the transfer start address to H'0 or H'08 in 16-byte unit access.