RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A084A/E	Rev.	1.00
Title	Notice of LVD circuit characteristics change (grade Y)		Information Category	Technical Notification		
Applicable Product	RL78/F13, F14 products (grade Y)	Lot No.	Reference Document	RL78/F13, F14 User's Manual: Hardware		
		All Lots				

Change of LVD circuit characteristics on RL78/F13, F14 products (grade Y) is shown below.

(1) LVD detection voltage of interrupt mode or reset mode

・ V_{LVD3} / V_{LVD4} / V_{LVD5} Maximum of Power supply rise time

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD3}	Power supply rise time	3.13	3.22	~~3.55~~ **3.66**	V
		V_{LVD4}	Power supply rise time	2.95	3.02	~~3.33~~ **3.44**	V
		V_{LVD5}	Power supply rise time	2.74	2.81	~~3.11~~ **3.22**	V

(2) LVD detection voltage of interrupt and reset mode

・ V_{LVD3} Maximum of Rising release reset voltage

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD3}	Rising release reset voltage	3.13	3.22	~~3.55~~ **3.66**	V

Please see the following pages.

Changing contents are shown as **gray hatching**.

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・ RL78/F13, F14 User's Manual: Hardware Rev.2.10 (R01UH0368EJ0210) P.1829

36.6.6 LVD Circuit Characteristics

[Before revision]

(1) LVD detection voltage of interrupt mode or reset mode

(T_A = -40 to +150°C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	4.62	4.74	5.22	V
			Power supply fall time	4.52	4.64	5.11	V
		V_{LVD1}	Power supply rise time	4.50	4.62	5.09	V
			Power supply fall time	4.40	4.52	4.98	V
		V_{LVD2}	Power supply rise time	4.30	4.42	4.87	V
			Power supply fall time	4.21	4.32	4.76	V
		V_{LVD3}	Power supply rise time	3.13	3.22	3.55	V
			Power supply fall time	3.07	3.15	3.47	V
		V_{LVD4}	Power supply rise time	2.95	3.02	3.33	V
			Power supply fall time	2.89	2.96	3.23	V
		V_{LVD5}	Power supply rise time	2.74	2.81	3.11	V
			Power supply fall time	2.68[Note]	2.75	3.00	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time		t_{LD}				300	µs

Note The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

(2) LVD detection voltage of interrupt and reset mode

(T_A = -40 to +150°C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 0, 1[Note 1], falling reset voltage: 2.75 V			2.68[Note 2]	2.75	3.00	V
	V_{LVD2}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		4.30	4.42	4.87	V
			Falling interrupt voltage		4.21	4.32	4.76	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 0[Note 1], falling reset voltage: 2.75 V			2.68[Note 2]	2.75	3.00	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		4.50	4.62	5.09	V
			Falling interrupt voltage		4.40	4.52	4.98	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1[Note 1], falling reset voltage: 2.75 V			2.68[Note 2]	2.75	3.00	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		3.13	3.22	3.55	V
			Falling interrupt voltage		3.07	3.15	3.47	V
	V_{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		4.62	4.74	5.22	V
			Falling interrupt voltage		4.52	4.64	5.11	V

Notes 1. These values indicate setting values of option bytes.

2. The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

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[After revision]

(1) LVD detection voltage of interrupt mode or reset mode

(T_A = -40 to +150°C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	4.62	4.74	5.22	V
			Power supply fall time	4.52	4.64	5.11	V
		V_{LVD1}	Power supply rise time	4.50	4.62	5.09	V
			Power supply fall time	4.40	4.52	4.98	V
		V_{LVD2}	Power supply rise time	4.30	4.42	4.87	V
			Power supply fall time	4.21	4.32	4.76	V
		V_{LVD3}	Power supply rise time	3.13	3.22	3.66	V
			Power supply fall time	3.07	3.15	3.47	V
		V_{LVD4}	Power supply rise time	2.95	3.02	3.44	V
			Power supply fall time	2.89	2.96	3.23	V
		V_{LVD5}	Power supply rise time	2.74	2.81	3.22	V
			Power supply fall time	2.68[Note]	2.75	3.00	V
Minimum pulse width		t_{LW}		300			µs
Detection delay time		t_{LD}				300	µs

Note   The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.

(2) LVD detection voltage of interrupt and reset mode

(T_A = -40 to +150°C, $V_{PDR} \leq EV_{DD0} = EV_{DD1} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 0, 1[Note 1], falling reset voltage: 2.75 V		2.68[Note 2]	2.75	3.00	V
	V_{LVD2}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.30	4.42	4.87	V
			Falling interrupt voltage	4.21	4.32	4.76	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 0[Note 1], falling reset voltage: 2.75 V		2.68[Note 2]	2.75	3.00	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.50	4.62	5.09	V
			Falling interrupt voltage	4.40	4.52	4.98	V
	V_{LVD5}	VPOC2, VPOC1, VPOC0 = 0, 1, 1[Note 1], falling reset voltage: 2.75 V		2.68[Note 2]	2.75	3.00	V
	V_{LVD3}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	3.13	3.22	3.66	V
			Falling interrupt voltage	3.07	3.15	3.47	V
	V_{LVD0}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	4.62	4.74	5.22	V
			Falling interrupt voltage	4.52	4.64	5.11	V

Notes 1.   These values indicate setting values of option bytes.

2.   The minimum value exceeds below the lower limit operation voltage (2.7 V), however, in reset mode, normal operation (same behavior when V_{DD} = 2.7 V) is possible until a reset is effected at the power supply falling time.