To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A567A/E	Rev.	1.00
Title	Notice for DREQ sampling in case of the split of DACK for external access		Information Category	Technical Notification		
Applicable Product	HD6417720 HD6417705	Lot No. ALL	Reference Document	SH7720 Hardware Manual (REJ09B0033-0200 Rev2.00) SH7705 Hardware Manual (REJ09B0082-0200O Rev2.00)		

For Applicable Product, there is a notice in DREQ sampling in case of the split of DACK for external access.

1. Content

There are cases that when DACK is split for an external access, DREQ can be sampled one time additionally in that access.

2. Conditions and Phenomena

Conditions: When DACK is split for an external access as following.

In the case of

(a) 16byte access or

(b) 32bit access for 8bit space or

(c) 16bit access for 8bit space or

(d) 32bit access for 16bit space

and the case of setting the idle cycle for

(i) Write-Write cycles (IWW[2:0]>=001) or

(ii) Read-Read cycles in the same spaces (IWRRS[2:0]>=001) or

(iii) External Wait Mask Specification (WM =0).

Phenomena: There are fig1. and Fig3. in next pages about DREQ sampling for above access.

DREQ can be sampled correctly except above access. (Fig2. snd fig4.)

3. Work around

When you use the external access as shown above 2.Conditions, please use the following note.

Note:

1) For DREQ edge detection: please input one DREQ edge at maximum in that external access.
2) For DREQ level detection in overrun 0: please negate DREQ after the detection of the first DACK negation and before the second DACK negation.
3) For DREQ level detection in overrun 1: please negate DREQ after the detection of the first DACK assertion and before the second DACK assertion.

4. Example of DREQ Input Detection

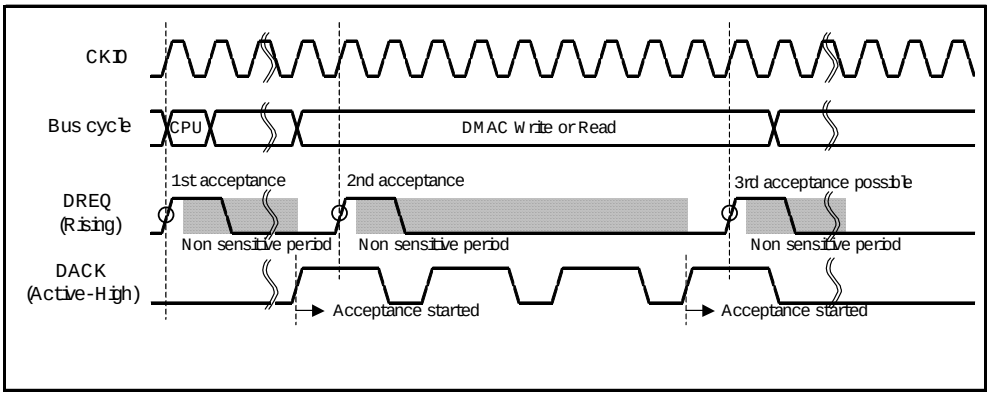

Fig1. Example of DREQ Input Detection in Cycle Steal Mode Edge Detection

When DACK is split to 4 due to Idle Cycles (Error)

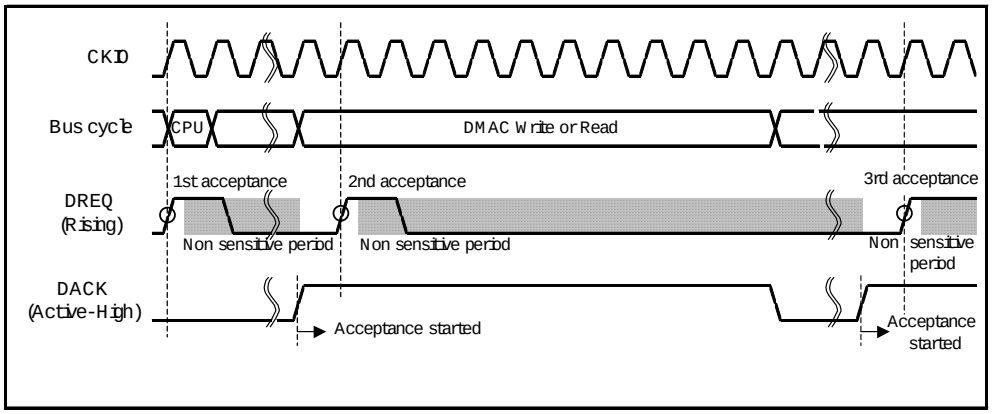

Fig2. Example of DREQ Input Detection in Cycle Steal Mode Edge Detection

When DACK is not split to 4 due to Idle Cycles (Correction)

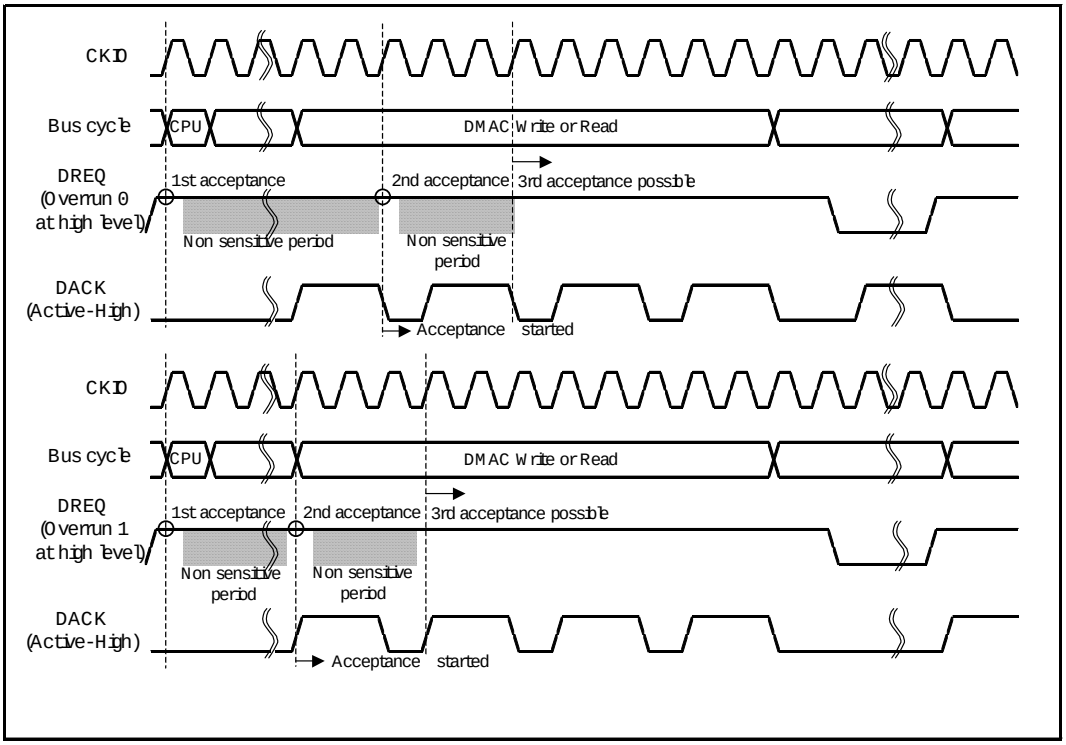

Fig3. Example of DREQ Input Detection in Cycle Steal Mode Level Detection

When DACK is split to 4 due to Idle Cycles. (Error)

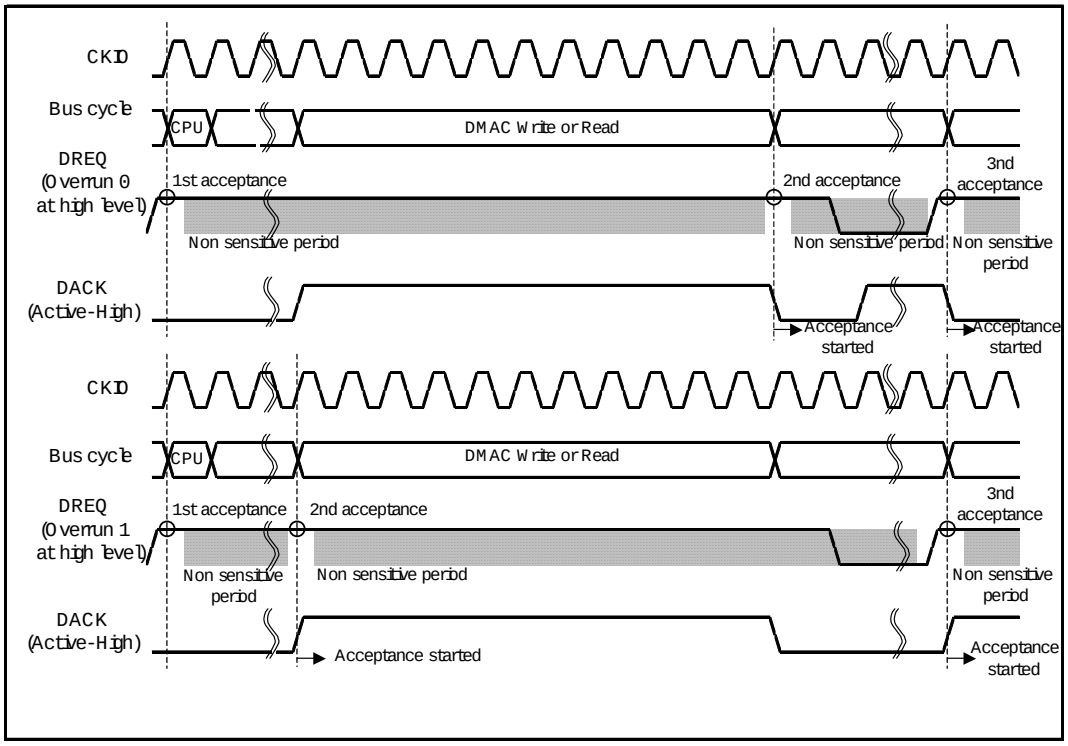

Fig4. Example of DREQ Input Detection in Cycle Steal Mode Level Detection

When DACK is not split to 4 due to Idle Cycles. (Correction)