To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-SH7-A644A/E	Rev.	1.00
Title	Notice and error correction about deep standby control register (DSCTR) and power-on reset exception handling.		Information Category	Technical Notification		
Applicable Product	R5S72650P200BG, R5S72651P200BG, R5S72652P200BG, R5S72653P200BG, R5S72050W200BG	Lot No. ALL	Reference Document	・SH7265 Group Hardware Manual Rev.1.00 (REJ09B0351-0100) ・SH7205 Group Hardware Manual Rev.1.00 (REJ09B0372-0100)		

We would like to inform you of the following notice and error correction about deep standby control register (DSCTR) and power-on reset exception handling in the above-mentioned applicable products.

1. Error correction

[Error] 35.3 (SH7265) / 32.3(SH7205) Register States in Each Operating Mode

Module Name	Register Abbreviation	Deep Standby
Power-Down Modes	DSCTR	Retained

[Correction] 35.3 (SH7265) / 32.3(SH7205) Register States in Each Operating Mode

Module Name	Register Abbreviation	Deep Standby
Power-Down Modes	DSCTR	Initialized

2. Notice

- The read value of bits 7 and 6 of deep standby control register (DSCTR) are undefined.

- After (1) power-on reset by /RES pin is released, (2) the LSI transit to deep standby mode in case that bit 6 (RAMBOOT) of deep standby control register (DSCTR) is set to “1”, (3) the deep standby mode is cancelled, and (4) power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again, then the behavior of the power-on reset exception handling is as follows.

Address where the program counter (PC) is fetched	Address where the stack pointer (SP) is fetched
H’FF800000	H’FF800004

So if applicable as above case, PC and SP are necessary to be retained in the area of on-chip RAM for data retention.

- After (1) power-on reset by /RES pin is released, (2) the LSI transit to deep standby mode, and (3) the deep standby mode is cancelled, if there is a possibility that power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again, the settings of WDT or H-UDI should be done in the condition that bit 15 (IOKEEP) and bits 9~0 of deep standby cancel source flag register (DSFR) are all cleared after canceling deep standby mode (if some bits are 1, please write these as “0” after reading these as “1”).

  If (1) the setting of WDT or H-UDI is done in the condition that IOKEEP bit is not 0, and (2) power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again, the pin status of the pins, whose pin status

are retained in deep standby mode and which are not in table 33.4 (SH7265) / table 30.4 (SH7205), are kept retained. Additionally, in the case that bit 7 (CS0KEEPE) of deep standby control register (DSCTR) are set to “1”, the pin status of the pins in table 33.4 (SH7265) / table 30.4 (SH7205) are also keep retained.

If (1) the settings of WDT or H-UDI is done in the condition that bits 9~0 are not all 0, and (2) power-on reset by WDT or H-UDI reset is occurred before power-on reset by /RES pin is executed again, the internal information about the deep standby canceling source is not cleared, and deep standby mode are cancelled by the wrong canceling source when the LSI attempt to transit to deep standby mode since then.