

# RENESAS TECHNICAL UPDATE

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Product Category	SRAM		Document No.	TN-M62-A139A/E	Rev.	1.00
Title	Notice about the generation change of 4Mbit LP SRAM series 5V version		Information Category	Product Generation Change		
Applicable Product	4Mbit Low Power SRAM 5V version; R1LP0408C series to R1LP0408D series	Lot No.	Reference Document	Nothing		
		All shipped lots after '12/4				

Please be informed that we, Renesas will be proceeding with the product generation change of 4Mbit LP SRAM 5V version from "R1LP0408C series" to "R1LP0408D series". This generation change is scheduled as follows.

"R1LP0408D series is fully compatible to "R1LP0408C series", from the electrical characteristics specifications and package dimension. So your acceptance of paper qualification and your kind understanding are greatly appreciated.

## <Generation Change>

This generation change is to shrink die with 0.15um technology, in order to improve the production efficiency.

All packages' outline is completely same.

We make use of Renesas original technology with adoption of memory cell with TFT load and capacitor structure for this part.

By adopting the original technology, we could offer an excellent high reliability against Soft error and latch-up phenomenon.

## <Objective parts>

4Mb (x8) 5V, SOP : from R1LP0408CSP series to R1LP0408DSP series

4Mb (x8) 5V, TSOP : from R1LP0408CSB series to R1LP0408DSB series

## <Document and Sample availability>

Data sheet : Available(Preliminary), Apr./2012(Rev.1.0)

CS sample : Mar./2012(R1LP0408DSP), Apr.2012(R1LP0408DSB)

Reliability report : Mar/2012(R1LP0408DSP), Apr.2012(R1LP0408DSB)

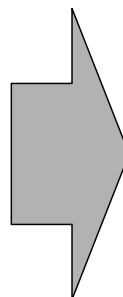
## <Launch date of this "generation change">

We will start shipping out new generation parts from April in 2012. There will be a possibility to ship out both current parts series (R1LP0408C) and new parts series (R1LP0408D) in parallel, because of our inventory of current parts series.

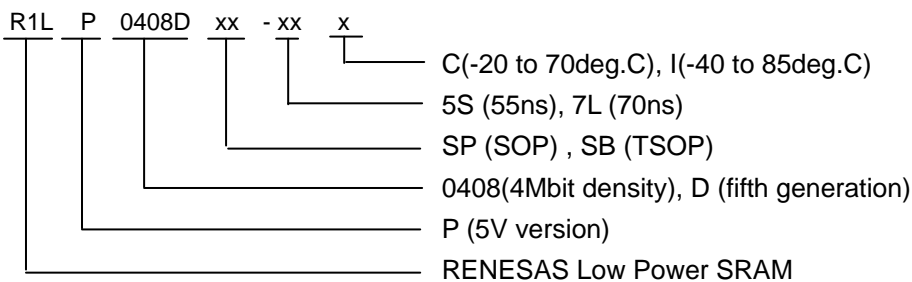
## <Replaced part name list on this generation change>

### 1) replaced part name on this generation change <4Mb Low Power SRAM (5V version)>

P/N	Package	Access Speed	Operating Temp.	P/N of new generation	Operating Temp.
R1LP0408CSP-5SC	SOP(32)	55ns	-20 to 70deg.C	<b>R1LP0408DSP-5SR</b>	0 to 70deg.C
R1LP0408CSP-7LC		70ns	-40 to 85deg.C	<b>R1LP0408DSP-7SR</b>	-40 to 85deg.C
R1LP0408CSP-5SI		55ns		<b>R1LP0408DSP-5SI</b>	
R1LP0408CSP-7LI		70ns		<b>R1LP0408DSP-7SI</b>	
R1LP0408CSB-5SC	TSOP(32)	55ns		-20 to 70deg.C	
R1LP0408CSB-7LC		70ns	-40 to 85deg.C	<b>R1LP0408DSB-7SR</b>	-40 to 85deg.C
R1LP0408CSB-5SI		55ns		<b>R1LP0408DSB-5SI</b>	
R1LP0408CSB-7LI		70ns		<b>R1LP0408DSB-7SI</b>	



**2) Explanation about part name**



Basically each correspondence follows the shown list, however we'd like to ask you all to check data sheet of new part.

**<Comparison between old parts series and new parts series>**

Circuit	R1LP0408C series	R1LP0408D series
Memory cell structure	Full CMOS cell	TFT load capacitor
Peripheral circuit	CMOS	CMOS

Process	R1LP0408C series	R1LP0408D series
Wafer process layer	1poly, 3metal, 1tungsten	8poly, 2metal, 1tungsten
Design rule	0.18 $\mu$ m	0.15 $\mu$ m
Gate oxide thickness	3.2nm(memory cell)/7.7nm(peripheral circuit)	6.5nm(memory cell)/12nm(peripheral circuit)
Gate oxide material	SiO <sub>2</sub>	SiO <sub>2</sub>
Passivation thickness	0.60 $\mu$ m	0.75 $\mu$ m
Passivation material	p-SiN	p-SiN

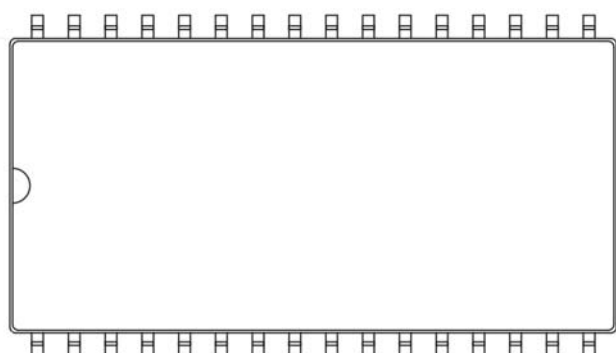
Assembly	R1LP0408C series	R1LP0408D series
Resin material	Epoxy	Epoxy
Lead frame material	Fe-Ni 42 alloy	Cu
Lead frame plating	Sn/Cu	Sn
Inner write material	Au	Au
Die bond material	resin	resin

**<Index mark specification>**

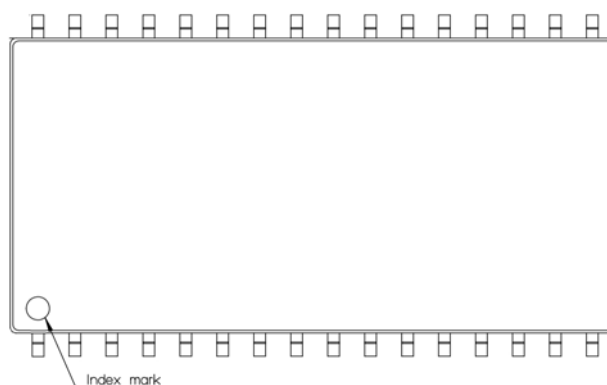
Index mark of TSOP package is changed as the following chart. Index mark of new version that is for R1LP0408DSB series shows first pin position.

Other marking specifications (Part name, Data code and etc.) are not changed.

<R1LP0408CSB Series (32P3Y)>



<R1LP0408DSB Series (32PTY)>



<Specification comparison of 4Mb low power SRAM(R1LP0408C series/R1LP0408D series)>

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Memory cell structure		Full CMOS Type			TFT load + capacitor cell	
Peripheral circuit		CMOS			<--	
Design rule		0.18um			0.15um	
Package		SOP 32pin(20.75mm x 14.1mm) TSOP II 32pin(20.0mm x 8mm)			<--	

DC condition

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Supply voltage	Vcc	4.5V to 5.5V		Vcc	<--	
Operating temperature range	Ta	5SC/7LC	-20deg.C to 70deg.C	Ta	5SR/7SR	0deg.C to 70deg.C
		5SI/7LI	-40deg.C to 85deg.C		5SI/7SI	<--
Input Voltage	VIH	2.2V(min.)/Vcc+0.3V(max.)		VIH	<--	
	VIL	-0.3V(min.)/0.8V(max.)		VIL	<--	

DC characteristics

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Average operating current	Icc1(TTL, Cycle=55ns)	25mA(max.)/8mA(typ.)		Icc1(TTL, Cycle=55ns)	25mA(max.)/15mA(typ.)	
	Icc2(MOS, Cycle=1us)	5mA(max.)/2mA(typ.)		Icc2(MOS, Cycle=1us)	5mA(max.)/3mA(typ.)	
Active standbu current	Icc(CS#=VIL)	3mA(max.)/1.5mA(typ.)		Icc(CS#=VIL)	10mA(max.)/5mA(typ.)	
Standby Current	ISB1(MOS input) (Vcc=5.5V)	ISB(TTL input)	0.5mA(max.)/0.1mA(typ.)	ISB(TTL input)	<--	
		up to 25deg.C	7LC/I: 10uA(max.)/0.8uA(typ.)	ISB1(MOS input) (Vcc=5.5V)	up to 25deg.C	2.5uA(max.)/0.8uA(typ.)
			5SC/I: 3uA(max.)/0.8uA(typ.)		up to 40deg.C	3uA(max.)/1.0uA(typ.)
			7LC/I: 10uA(max.)/1.0uA(typ.)		up to 70deg.C	8uA(max.)
			5SC/I: 3uA(max.)/1.0uA(typ.)		up to 85deg.C	10uA(max.)
up to 70deg.C	7LI: 20uA(max.)					
up to 85deg.C	5SI: 10uA(max.)					
Output Voltage	VOH	IOH=-1.0mA	2.4V(min.)	VOH	<--	
		IOH=-0.1mA	2.6V(min.)		<--	
		IOL=2.1mA	0.4V(max.)		<--	
	VOL			VOL	<--	

Capacitance

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Input capacitance	Cin	8pF(max.)		C in	<--	
Input/Output capacitance	C I/O	10pF(max.)		C I/O	<--	

AC characteristics

Read Cycle

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Read cycle time	tRC	5SC/5SI	55ns(min.)	tRC	5SR/5SI	<--
		7LC/7LI	70ns(min.)		7SR/7SI	<--
Address access time	tAA	5SC/5SI	55ns(max.)	tAA	5SR/5SI	<--
		7LC/7LI	70nm(max.)		7SR/7SI	<--
Chip select access time	tCO	5SC/5SI	55ns(max.)	tACS	5SR/5SI	<--
		7LC/7LI	70nm(max.)		7SR/7SI	<--
Output enable to output valid	tOE	5SC/5SI	25ns(max.)	tOE	5SR/5SI	<--
		7LC/7LI	35ns(max.)		7SR/7SI	<--
Chip select to output in low-Z	tLZ	5SC/5SI	10ns(min.)	tCLZ	5SR/5SI	<--
		7LC/7LI	10ns(min.)		7SR/7SI	<--
Output enable to output in low-Z	tOLZ	5SC/5SI	5ns(min.)	tOLZ	5SR/5SI	<--
		7LC/7LI	5ns(min.)		7SR/7SI	<--
Chip deselect to output in high-Z	tHZ	5SC/5SI	0ns(min.)/20ns(max.)	tCHZ	5SR/5SI	<--
		7LC/7LI	0ns(min.)/25ns(max.)		7SR/7SI	<--
Output disable to output in high-Z	tOHZ	5SC/5SI	0ns(min.)/20ns(max.)	tOHZ	5SR/5SI	<--
		7LC/7LI	0ns(min.)/25ns(max.)		7SR/7SI	<--
Output hold from address change	tOH	5SC/5SI	10ns(min.)	tOH	5SR/5SI	<--
		7LC/7LI	10ns(min.)		7SR/7SI	<--

Write Cycle

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Write cycle time	tWC	5SC/5SI	55ns(min.)	tWC	5SR/5SI	<--
		7LC/7LI	70ns(min.)		7SR/7SI	<--
Chip selection to end of write	tCW	5SC/5SI	50ns(min.)	tCW	5SR/5SI	<--
		7LC/7LI	60ns(min.)		7SR/7SI	<--
Address setup time	tAS	5SC/5SI	0ns(min.)	tAS	5SR/5SI	<--
		7LC/7LI	0ns(min.)		7SR/7SI	<--
Address valid to end of erte	tAW	5SC/5SI	50ns(min.)	tAW	5SR/5SI	<--
		7LC/7LI	60ns(min.)		7SR/7SI	<--
Write pulse width	tWP	5SC/5SI	40ns(min.)	tWP	5SR/5SI	<--
		7LC/7LI	50ns(min.)		7SR/7SI	<--
Write recovery time	tWR	5SC/5SI	0ns(min.)	tWR	5SR/5SI	<--
		7LC/7LI	0ns(min.)		7SR/7SI	<--
Write to output in high-Z	tWHZ	5SC/5SI	0ns(min.)/20ns(max.)	tWHZ	5SR/5SI	<--
		7LC/7LI	0ns(min.)/25ns(max.)		7SR/7SI	<--
Data to write time overlap	tDW	5SC/5SI	25ns(min.)	tDW	5SR/5SI	<--
		7LC/7LI	30ns(min.)		7SR/7SI	<--
Data hold from write time	tDH	5SC/5SI	0ns(min.)	tDH	5SR/5SI	<--
		7LC/7LI	0ns(min.)		7SR/7SI	<--
Output active from end of write	tOW	5SC/5SI	5ns(min.)	tOW	5SR/5SI	<--
		7LC/7LI	5ns(min.)		7SR/7SI	<--
Output disable to output in high-Z	tOHZ	5SC/5SI	0ns(min.)/20ns(max.)	tOHZ	5SR/5SI	<--
		7LC/7LI	0ns(min.)/25ns(max.)		7SR/7SI	<--

Data retention characteristics

Item	Symbol	R1LP0408C series		Symbol	R1LP0408D series	
Vcc for data retention	VDR	2.0V(min.)		VDR	<--	
Data retention current	IccDR (Vcc=3.0V)	up to 25deg.C	7LC/I: 10uA(max.)/0.8uA(typ.) 5SC/I: 3uA(max.)/0.8uA(typ.)	IccDR (Vcc=3.0V)	up to 25deg.C	2.5uA(max.)/0.8uA(typ.)
		up to 40deg.C	7LC/I: 10uA(max.)/1.0uA(typ.) 5SC/I: 3uA(max.)/1.0uA(typ.)		up to 40deg.C	3uA(max.)/1.0uA(typ.)
		up to 70deg.C	7LC/I: 16uA(max.) 5SC/I: 8uA(max.)		up to 70deg.C	8uA(max.)
		up to 85deg.C	7LI: 20uA(max.) 5SI: 10uA(max.)		up to 85deg.C	10uA(max.)
		Chip deselect to data retention time	tCDR		0ns(min.)	
Operation recovery time	tR	55ns/70ns(min.)		tR	5ms(min.)	

Sincerely yours.